Integration of Education and Research in Microelectronics

Workshop Proceedings

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Introduction

Educational use of MOSIS (Metal-Oxide Semiconductor Implementation Service) has been credited as being a crucial element in establishing excellence in computing and communications in the U.S. [1]. On March 29, 1996 a workshop was held at NSF to assess the status and future trends of the educational use of MOSIS.

This workshop was the first major meeting of users of the NSF/ARPA supported Educational MOSIS since the 1993 Workshop on Rapid Prototyping of Microelectronic Systems for Universities [2]. That Workshop adopted the following vision statement.

Educate students who can use the paradigm of design, simulate, design-for-test, build and test (as opposed to just design, build and test) to create microelectronic systems, not just integrated circuits, of sufficient quality that the global competitiveness of U. S. industry will be continued and enhanced.

To implement the vision, the workshop endorsed the following principle.

Rapid prototyping of microelectronic systems should be an integral part of the education process since students must have the experience of taking a design from initial specifications to a working implementation.

Over the intervening three years educational use of MOSIS has implemented the vision by providing access to the MOSIS Service to all qualified educational users. By the end of 1995 almost three hundred class accounts have been established and VLSI has become a vital component of technical university education, not just in Computer Engineering, but all aspects of circuit and electronic systems design. In all institutions advanced undergraduate electronics and computer system education relies heavily on tools devised for VLSI fabrication and verification AND in all institutions the application of VLSI and MOSIS techniques has strongly bonded the educational and research activities of the participating faculty and students.

At the current workshop eighteen invitees, representing a crossection of educational users of MOSIS, met to discuss

1. Role of VLSI and MOSIS in an educational setting.
2. Role of fabrication and simulation in VLSI education.
3. Role of MOSIS in VLSI Education.
4. Strengthening the Educational MOSIS community.

The invitees were asked to prepare a statement summarizing their own activities in VLSI education and their experiences. These position papers are attached.

Goals of the Workshop

The goals of the workshop are to develop recommendations in the effective use of MOSIS for beginning and advanced classes. The following is a list of questions considered.

A. Role of VLSI and MOSIS in an Educational Setting

A1. Where is MOSIS used? Where should it be used?

A2. What is the educational value of MOSIS for schools?

B. The Role of Simulation and Fabrication in VLSI education

B1. What is the educational value of a completed design (hard chip)?

B2. Do we really need to fabricate chips for elementary classes?

B3. To what extent should virtual prototyping be used, especially in beginning classes?

C. MOSIS in VLSI Education

C1. How does group size influence the educational value to the student of the MOSIS experience?

C2. To what extent should the success rate of instructors' classes affect the priorities and funding of their subsequent classes?

C3. What should the chip reports contain?

C4. How should reports be accessible to others?

C5. What does testing contribute to the designer's education?

D. The MOSIS Community

D1. Funding is tight, and likely to remain so for the foreseeable future. What steps may be taken to maintain and enhance the educational values MOSIS provides to US technical strength?

D2. It may be possible to organize an electronic bulletin board for Educational MOSIS. This would be a chiefly student/student information sharing network. What actions would be appropriate in this respect? How would such a network benefit the student and generate enthusiasm, better reporting and testing?

Background

The Metal-Oxide Semiconductor Implementation Service (MOSIS) [3] provides three types of accounts: commercial, research and education. The latter has enabled educational users access to the manufacture of communication and computer engineering circuit and systems designs. Every school is eligible to apply for an education account; the only requirements are that instructors are qualified and that appropriate design and testing facilities exist. Submission of completed designs is typically through the Internet, and completed chips are returned by priority mail. The MOSIS service has been credited with enabling the USA to produce enough computer hardware designers to establish a national supremacy in the development of computers and communications [1]. MOSIS has been funded by the Advanced Research Projects Agency since 1981 and for the last 6 years it has been jointly funded by ARPA and the National Science Foundation. During the last 15 years over 25,000 projects have been completed. MOSIS is available for classes, as well as research and development projects and grants. This Workshop was concerned with the use of MOSIS by classes .

Currently the educational use of MOSIS is about 10% of the total budget of MOSIS. Educational designs from classes amount to about 50% of all fabricated chip designs. Every year about 5000 students in over 180 classes receive much of their computer engineering design experience through MOSIS. This is estimated to be about 40% of all computer engineering students. In addition some schools have their own fabrication facilities. There are two types of classes that NSF supports: beginning (about 110 classes) and advanced (about 75 classes). All of the numbers mentioned are approximate: the MOSIS service is a dynamic entity, with clients being added daily and those who completed their academic training dropping off the client list. Perhaps 3000 eventual industrial hardware designers per year receive their introduction to microelctronic systems and computer engineering through this service.

Academic users simply formulate circuit designs and submit them to the MOSIS broker in a standardized form. The broker currently is ISI (Information Sciences Institute of the University of Southern California.) The broker consolidates the designs into wafer-sized fabrication runs and submits these for fabrication. Fabrication is accomplished by commercial fabricators (fab houses), with whom ISI arranges for an affordable cost. Fabrication facilities are very expensive; a commercial facility may be a 2.5 billion dollar investment.

The basic unit of manufacture is a wafer, typically having a 4 or 8 inch diameter area, on which circuits are grown. The broker combines many different designs (often over a hundred), which originates in different classes, projects and commercial users. In this way the large overhead may be shared, thus affording a capability for educational institutions to make use of modern electronic manufacturing and enabling the institutions to teach modern design methods up to and including the fabrication of the designs and their testing.

The basic use of educational MOSIS is that students will take a basic course, typically the second or third course in computer hardware or in communications. However, in some schools MOSIS supports all electronics design classes, starting from the very first electronics design class through the advanced computer and communication system graduate courses. There exist a number of excellent textbooks which provide a thorough introduction to the underlying theory and practices. Foremost among these is ‘the Mead-Conway book’ [4].

MOSIS is a service that brings modern electronic design tools and fabrication facilities to academic research endeavors and design experience to technical students. MOSIS provides a number of fabrication modes; each designer is expected to start with relatively uncomplicated designs with well-established technologies and may then progress to more

complex designs in advanced classes or with individual projects. The basic design classes are allocated funds sufficient to fabricate one TinyChip in 2 um CMOS technology for each group of two students. A TinyChip is an area of approximately 2500 um by 2500 um (2.5 by 2.5 millimeters, about 1/10 inch square). The 2 um CMOS technology allows about 600 'features' to be put in each direction on the surface of the chip; features may be connection wires or parts of a transistor device. Students may design any circuitry that fits on that area. This area is small compared to current commercial micro-electronic devices; a Pentium microprocessor requires about 100 times that much area. Nevertheless, there is enough space on a TinyChip to design electronic systems with over 4000 transistors. The complexity of such a design is larger than any other design the student would otherwise encounter in a college experience. The designs must follow standardized design rules [5].

The normal allocation is one TinyChip per two students for Beginning Classes, and one TinyChip per student for Advanced Classes. Upon special application, justification, and approval, it may be possible to fabricate with finer feature sizes and/or larger chip areas.

The students' designs are submitted to the MOSIS broker electronically in forms acceptable to the fabricator; overwhelmingly this is CIF format (CalTech Intermediate Form), which has become a means of international information exchange for integrated electronics. The students are expected to design, simulate, design tests, and complete testing after fabrication for computer and/or communication sub-sections using public domain (or commercial) software packages. Thus the students are exposed to the whole cycle of a non-trivial design experience, often the only one they will get in their academic studies. A design project fabricated under the auspices of MOSIS ends with the submission of a cryptic report from which usage data and gross success/trouble data can be gleaned. Since the summer of 1995 a one/two page precis was also required; recent MOSIS Project Reports do contain such descriptive material.

In January 1995 a new database was established to track the Project reports. The data represents a snapshot of MOSIS, but a necessarily blurry one. Since the average time between submission of a chip design and the testing of the fabricated chip is 23 weeks, it is difficult to establish an up-to-date picture of the state of MOSIS short of accounting for every design. Classes form, schools apply for accounts, and some become dormant for a term (or more). What is considered are the class account applications, the class budgets at the beginning and end of the yearly funding cycle (October 1 through September 30) and the individual Project Reports. The following numbers report information for the period January 1, 1995 through January 24, 1996.

At the beginning of FY 1995 there were 288 educational accounts. Not all were active. Active were

110 Beginning Class accounts (4038 students);

77 Advanced Class accounts (950 students).

The number of designs submitted for fabrication during this slightly over a year period were:

948 Beginning Class designs;

238 Advanced Class designs.

There were 556 chips reported tested. About half of the chips tested during this period were designed in 1994, and chips fabricated during the latter half of 1995 will be tested at later times.

70% of all fabricated designs were reported 'performs as designed or better'.

There were 4038 students in all Beginning Classes, and initially about 2020 chips were budgeted. Historically many designs envisioned at the beginning of a term are not submitted for fabrication (due to missed deadlines, errors discovered during simulation, improved designs conceived during initial design, and student drop-outs.) During this period there were 948 chip designs submitted for fabrication (35% of targeted.)

The average cost per Beginning Class design (nominally a TinyChip per two students) was $500. Normally four copies are made for each design. For Advanced Classes the budget is one TinyChip per student. On the average about 53% of the requested budget was used in Advanced Classes, and about 40% in Beginning Classes. For Advanced Classes the cost per completed design was $1100.

The Chip Report Database lists for each submitted design information about design submission date, testing date, and cursory test results. The data is derived from the fabrication reports from ISI and the MOSIS Project Reports. Data for submitted designs are compiled with the test reports for each individual project.

During this period some 1100 chip designs were submitted for fabrication and 560 chips were tested and reported, for a report-rate of about 50%. Additional test reports are expected. Often test reports are not submitted until the class account needs to be re-activated (typically a year later.) Meanwhile students may leave, chips may be displaced and reports may be incomplete. The average time for submission of the design to completion of the report is 23 weeks. There is an inherent two-week inaccuracy in the data: the fabrication time is taken to be the last day of the month of actual fabrication.

On the average, about 70% of the designs are reported as meeting or exceeding the design specifications. In many instances the test instrumentation is inadequate, particularly for high-speed designs or accurate analog designs. Information about the instrumentation problems is sometimes in the comments that appear in many of the Project Reports.

Digital vs. Analog Designs. Since late 1994 all fabrications done through MOSIS were CMOS analog, even though most designs were standard on-off logic circuits. The major reason is that there are not enough pure-digital designs, and mixing analog and digital circuits for fabricating only one type of circuit in the same fabrication run results in lower costs. Logic designs fabricated on analog circuit production lines work just fine.

Training per Design Project. Funding level for a beginning class is for two students per TinyChip. The main reason for this mode of support is the desirability to give each student an opportunity for acquiring a realistic design experience, including the problem formulation, system decomposition, circuit design, layout generation, and all test phases. Group dynamics indicate that often teams of three split thus impeding learning and design efficiency, but single-person designs miss the essence of team work. Hence the support level for beginning classes was pegged at a group of two persons per chip design. However, the data shows that only about 35% of the number of designs anticipated at the beginning of the term are actually submitted. Hence in reality there were about 6 students for each completed and tested design.

The various position papers list courses, design packages used by the various classes, as well as validation and verification tools used. As a rule classes use Public Domain software (which is available through MOSIS or by word-of-mouth) or industrially donated large CAD packages.

In the following there willl be some repetition of information already presented. This is done in an effort to make the various sections self-contained.

Findings

General. Every school may use the MOSIS fabrication facilities. Two types of accounts are supported: beginning classes (110 in FY95) and advanced classes (77 in FY95). There are 288 educational accounts, but not every instructor teaches microelectronics systems or computer system design classes every year. Applications for new accounts are received continuously. In FY96 there were approximately 4000 students in the beginning classes and about 950 in the advanced classes. **MOSIS is the premier NSF grant in the integration of education and research**.

Since the summer of 1995 the project reporting requirements have included a short precis which describes the design goals, the design and the test results. Previously no data was collected on these; the new reports need to be summarized and the information needs be extracted into a useful form. A new data base was established starting with the January 1995 Project reports.

Project Precis. The Project Report forms provide space for five lines of written comments. Since the Spring 1995 a one/two page short report has been requested. Not all classes submit a short report as yet. Apparently some instructors are not heeding the request for information to explain the project; the vast majority of reports received include no material beyond cursorily filling-in the long-established form.

The few that do contain a one/two page summary are very interesting. They show a wide range of application for these chips, including simple counting circuits, modest microprocessors, various instruments and sensors, communication devices, biomedical devices, as well as various computer hardware sections. The short reports document a wide variety of technical topics, fully mirroring the range of applications of modern microelectronics and computer devices. A systematic taxonomy of these applications need to established to smoothly track the deep influence MOSIS has made in all aspects of electronic technology.

Project Ideas. Often class designs are very similar, perhaps duplicates, even in classes located half-way across the country. Instructors need example cases for classes. The appropriate size of a project is difficult to estimate without extensive experience and/or detailed examples.

Design and Verification Tools. All classes use extensive CAD tools. Many are in the public domain (for example MAGIC), others are commercial packages ranging from extensive and expensive (for example Verilog) to modest (such as Tanner Tools.) Verification tools are similarly eclectic; some are more precise than others. Common difficulties in circuit verification include difficulties with parasitic diodes, insufficient ground and power.

Test Procedures. Testing is an afterthought, not systematic work. The degree to which testing is included in the design phases depends largely on the individual instructor. There is a need to acquaint instructors with Design-for-Test ideas, the need for extensive testing, and dynamic tests.

Test Equipment. Test jigs are needed, test instruments for functional tests (In/Out bit streams); test for speed; rise/fall time tests; load tests; reliable high-speed clocks are needed. As clock speeds rise better instrumentaion is required. In many schools the teaching functions rely heavily on the locally available research instrumentation.

Instructor Training. New instructors need help; class success rate depends strongly on the instructor. Many instructors learned VLSI design from a set of video tapes based on a short course originally given at Cal Tech and Xerox. These tapes are still a valued resource, but they need to be updated. Similarly an on-call expert is needed who instructors could contact periodically.

Virtual Prototyping. Some schools do not fabricate designs in beginning classes, just do intensive simulation tests (extensive use of Validation & Verification programs and SPICE). In fact only about 40% of the Beginning Class designs, and 53% of the Advanced Class designs are submitted for fabrication. There are several reasons for this:

1. Students fail to complete the class. We do not have data on just what the class completion rate is, but there are also add-ons after the registrar's 'official' class-lists, based on average class drop-outs this is estimated at 5%.
2. Class projects may be combined.
3. Designs are not completed. Students tend to overestimate their productivity (and underestimate the complexity of system designs.) Some students just drop the course, thus falling into category 1, above; others simply complete the course at a later opportunity.
4. Simulation results. The design of a MOSIS chip basically produces a geometrical description of at least three layers of electrically active parts, the 'masks' used in producing the physical chip. These mask descriptions, combined with accurate descriptions of the chip manufacturing process, can be used to extract component behavior and thus provide an accurate description of the underlying electronics. The action of the electronics can then be calculated accurately, thus providing a reading of what the fabricated chip would do.

   It is required to extensively simulate each chip before submission for fabrication to MOSIS. Often design errors and omissions are discovered at this stage, and sometimes an examination of the simulation results reveals better design choices. Thus many designs are taken only to this stage, having served as a teaching vehicle for the introduction of the VLSI design cycle to yet another group of students. Indeed in some schools NO FABRICATION is done in the first class, only the design and simulation tools are introduced and practiced.

We do not accurately know the reasons for design incompletion; however, the use of extensive simulation is the predominant factor in keeping the MOSIS design submissions to an economically manageable level. The simulation tools take into account the fabrication parameters; thus the simulation of a design amounts to a process of virtually prototyping a chip. From a digital description of the mask geometry AND a database describing the manufacturing line, the designer is handed a computer file that very accurately describes the signals at every point of interest in the chip. The effects of manufacturing inaccuracies can be accounted for, and the fidelity of the circuit relative to the design specifications can be accurately predicted.

Over the last few years the simulation tools have become more accurate, signals can be ever more accurately calculated, and success/failure of the design can be accurately assessed. It is important to note that simulation can be carried out on the same computer system as the design itself; there is no need to wait for fabrication schedules and availability. Of course, simulation is far cheaper than fabricating.

Recommendations

The following recommendations from the Workshop were formulated at the conclusion of the meeting and by e-mail exchanges and visits over the ensuing four months.

1. Educational-MOSIS needs to be continued. In all US universities this has become an essential part of all Computer Engineering educational efforts, with about 40% of all USA university students in microelectronics and computer systems engineering directly preparing, submitting and testing designs, or using the VLSI design and verification tools.
2. Training courses for instructors. When Educational MOSIS started, a number of very successful, well-received summer classes were held for would-be instructors. Presently many new instructors are starting VLSI classes. It is recommended to implement training for instructors, both new and those wanting a review. It would be very helpful if the original VLSI start-up classes, or a video-taped version, would be available with updated resource materials and representative complete designs.
3. An Educational-MOSIS Retrospective. There is much anecdotal testimony about the wide-spread use of Educational MOSIS for Computer Engineering and Microelectronics university training. Many students have gone on to jobs because of the program, and several have developed major technical enterprises directly credited to Educational MOSIS. It is recommended that a careful retrospective study of the impact of MOSIS be done, and data be collected about the value of Educational MOSIS.
4. Finer-line Geometries. Currently Educational MOSIS is budgeted for 2 um geometries. Over the last few years cell libraries have become available that enable higher-level design activities. The libraries are for finer geometries, typically 1.2 um or less. Many classes, especially Advanced Classes, already request fabrication of finer geometry designs. In order to make the library-based design tools more widely useful, especially for Beginning Classes, it is recommended that easier access to 1.2 um (and possibly finer) geometries be made available. It is understood that the possible increase in costs may require a change in the basic composition of design teams (going to 3 or 4 students, away from the present 2 students per design team.)
5. Increased Freedom of Fabrication Choices. Beyond Recommendation 4 (Finer-line Geometries) it is also recommended that instructors be given more freedom in choosing chip sizes and be allowed to include in their class accounts other MOSIS-supplied services. This is seen as a way for instructors and their classes to become more efficient in employing MOSIS offerings and to widen the educational experience for the classes.
6. Design-for-test. Many designs are undertaken without regard to adequate testing of the fabricated chip. Increasingly textbooks introduce this vital topic, but additional incentives should be made to have each design go through a rigorous Verification and Validation test. In this respect the Design and Test program of MIPS and the Educational MOSIS programs should co-operate more fully.
7. Virtual Prototyping. A full design may be accurately tested by producing a CIF file for fabrication, and then using the CIF file to extract the circuit (including realistic parameters for circuit parasitics, clock and power distribution nets) for input to powerful verification and validation tools. Widely used V&V software includes IRSIM, Berkeley SPICE and H-Spice. For many Beginning Classes this cycle (without actual fabrication and testing of a completed chip) is time-effective and provides sufficient learning experience. Fabrication of a hard chip is often mainly a motivating factor; the design experience can be accomplished in this virtual environment. As more powerful CAD and V&V tool become available on personal-computer based workstations this virtual prototyping mode may become much more widely used, since a variety of fabrication variables can be accurately simulated. One could thus teach a deeper understanding of the VLSI realization cycle.

8. Test Instrumentation. VLSI circuits fabricated through the educational use of MOSIS have increasingly become much faster and much more analog. The testing of such circuits, even if mounted in the standard MOSIS dual-in-line packaging requires fine instrumentation. Most teaching facilities do not have adequate instruments to carry out and record data on high-speed circuits. Instrumentation is missing for rise/fall time determination, loading effects, and adequate test sequences. This is seen as a challenge to the Research and Instructional Instrumentation Program normally overseen by NSF.
9. Allow Experimentation in Class Presentation. Presently MOSIS class accounts are budgeted for 2 um TinyChips. For Beginning classes two students per design are budgeted; and Advanced Classes budget one student per design. It is recognized that some instructors may wish to have alternative design team compositions and basic technologies. It is recommended that such experimentation be considered routine, consistent with the budgetary constraints implied by the present funds allocation scheme. Further, it is recommended that all changes be carefully documented, especially the pedagogical effects.
10. Establish an Internet-based Consortium . There is a need to share of design experiences, design tool evaluations, design and testing data, and education-oriented lore in VLSI activities. The existing co-operation and competition between the VLSI design classes at the University of Utah and at the University of Michigan may serve as an example for the details of this activity. Essentially such a network activity may strengthen all MOSIS users by enhancing the educational activities and helping in setting up a uniform training platform. In essence, active participants would help bring along others, thus providing a 'sweat equity' from the user community. There is a need to keep the various I/O pad frames and PLA templates up to date. This is expecially true for the public domain design tools used by a large number of universities.
11. Extension to MCMs. Various Advanced Class projects involve the design of individual chips which collectively make up a Multi-Chip Module. Interconnection is currently handled by the MIDAS service, also serviced by the same contractor (ISI) as the Educational MOSIS. It is recommended that MIDAS services should be more freely accessible to such classes in order to stimulate more complete system design activities for Microelectronic Systems and Computer Engineering. Possibly a method for field-modifiable MCM substrates should be found.
12. Extension to MEMs. The ARPA-supported MUMPS project allows the fabrication of Micro-Electro-Mechanical parts. Chiefly these items are tiny mechanical parts with a small amount of electronics. In order to facilitate larger MEM systems, it is recommended that access be provided for MUMPS-like services. It was also recognized that this may require substantial additional funding, and thus may not be achievable in the near future.

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APPENDIX

Materials Supplied by the Contributors

prior to the Workshop meeting

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1. Courses and Tools Used:

At the University of Cincinnati, the VLSI sequence has the following courses:

(1) Physical VLSI Design;
(2) VLSI Systems Design;
(3) Physical Design Automation; and
(4) VLSI Test and Validation.

These four courses, along with a year-long senior project in VLSI design and two other elective courses related to VLSI constitute the VLSI Systems Engineering minor program for majors in Electrical Engineering and Computer Engineering. Each of the above four courses are dual-level courses (senior undergraduate and first year graduate students may take them). Enrollment in each course is limited to 20 students; we usually grant exceptions and end up with about 30 students in each course. About half of these are undergraduate students. The actual demand (especially for the Physical VLSI Design course) is probably twice as much.

We use the following tools in the courses:

(1) Physical VLSI Design: Magic, IRSIM, Spice, mpla

(2) VLSI Systems Design:

(a) FPGA Tools: ViewLogic Schematic Capture, Xilinx XACT, ABEL compiler, Synopsys FPGA Compiler.

(b) ASIC Tools: Lager IV tools and/or Mentor GDT tools.

(c) Hardware: Xilinx FPGA prototyping boards.

(3) Physical Design Automation: standard Unix software development tools; no VLSI design tools.

(4) VLSI Test and Validation:

(a) Hardware: HP 16500A Logic Analysis Systems

(b) Software: USC TGS system, TSSI Software to exercise the ATE from Sun workstations.

2. Whether you encourage the actual fabrication of designs for beginning classes:

I strongly encourage the actual fabrication of designs, especially for the beginning classes, provided that the chips can be tested against the design specs by the same group of students.

3. What experiences you have in integrating research and education in your use of MOSIS:

Our graduate students interested in VLSI design and CAD research are trained through the VLSI course sequence.

We have used MOSIS services in research activities in our projects (sponsors: ARPA, Air Force, NASA, General Electric, etc.), funded projects on high-level synthesis, physical DA and VLSI design. Uses included fabrication of CMOS digital and analog chips (2 and 1.2 micron) and GaAs devices.

MOSIS experience certainly gave the right mind-set to our graduate students in conducting research in VLSI design and test tools.

4. What suggestions for future services you may have that would enhance the interest in use of MOSIS.

- Reduction of fabrication turn-around time if possible (to 3 weeks?).
- Shared test services
- Software sharing over Internet, in future.
- PCB development support (parts and fab).
- Sharing of project ideas and design/test reports for interesting projects.
- Perhaps, a biennial symposium of MOSIS educators to facilitate the above.

A. Role of VLSI and MOSIS in an Educational Setting

A1. Where is MOSIS used? Where should it be used?

At the University of Cincinnati, we use it in introductory courses (Physical VLSI Design in ECE and VLSI Design I in CS). We are usually content with virtual prototyping (simulations) in advanced courses. This is due to the reason that the students in advanced courses will not be around to test the chips if we had sent them for fabrication.

Designed chips should be post-fab tested, for both function and performance, whenever possible. MOSIS facilities can be used whenever it is possible to test the chips against the specifications.

A2. What is the educational value of MOSIS for schools?

Realism. Virtual prototyping is often too far removed from reality to replace real fabrication and test experience. Experience of testing a fabricated device against specs and for manufacturing defects is invaluable.

B. Fabrication vs. Simulation

B1. What is the educational value of a completed design (hard chip)?

Same as in A2 above. It has no value if the students are not required to test the fabricated chips.

B2. Do we really need to fabricate chips for elementary classes?

Yes. Often that's the only class where undergraduate students get an opportunity to design a chip, send it for fabrication and have it come back for testing before they graduate. Even if a senior undergraduate student takes an advanced course and designs a chip and sends it to fab, it may not come back on time for her to test it.

B3. To what extent should virtual prototyping be used, especially in beginning classes?

If the fabricated chip is not going to be tested, then virtual prototyping may be sufficient. If it is going to be tested by the same student that designed it, then it is of great educational value and should not be replaced with virtual prototyping whenever possible.

I think, especially in the beginning classes real fabrication and testing brings enough realism to the students that more advanced classes (using the same technology) may use virtual prototyping.

C. MOSIS in VLSI Education

C1. How does group size influence the educational value to the student of the MOSIS experience?

Two students per project team seems to work well. I don't have good experiences with more than two students per project team. It seems to diminish the educational experience of the students, including the MOSIS experience.

The issue of students per project team is somewhat different in my mind from the issue of the number of chips per student (0.5 currently) approved by NSF/ARPA. For example, it may be possible to have two students per team and share one chip per two project teams (especially at 1.6 or 1.2 microns) and still retain the same educational value. However, my preference would be to provide one chip per project team and two students per project team.

C2. To what extent should the success rate of instructors' classes affect the priorities and funding of their subsequent classes?

It depends on what the ``success rate of an instructor'' is and how one measures it. In general, I think there should be some accountability. Current process requires filing of the test reports. It is not clear if these reports are reviewed in any way. May be these would be sufficient, if they are more structured and if there is some review process.

If we can evolve a reasonable definition of success of an institution or instructor in using MOSIS to enhance the educational experience of the students (taking into account student attrition, changes in instructor-course assignments and other logistics) and a reasonable report format for documenting this evidence then NSF/ARPA may be able review and use these for future funding decisions. Reviewing the reports may be a big task as well

considering that 195 or so universities use MOSIS. May be each institutional representative needs to `volunteer' to review 1-3 other universities' reports and make a recommendation based on CLEARLY AND OBJECTIVELY DEFINED CRITERIA.

Review process should be structured to encourage and foster proper use of the MOSIS experience, not to discourage and dissuade. Last thing we want to do is to establish a process that would routinely eliminate resource-strapped universities from the MOSIS user list.

C3. What should the chip reports contain?

Several things come to mind: (1) summary of the design function; (2) performance goals; (3) Pin-out and I/O protocol; (4) `users manual' of the chip; (4) test methodology and tools; (5) functional testing and results; (5) performance testing and results; (6) evaluation summary.

These are items that we expect to write in their class reports on chip testing. The same items, perhaps in a more condensed form and structured format, should be in the reports to MOSIS as well. I wonder if these need to be in hard-copy form or simply made available through MOSIS activities home pages maintained at each university.

C4. How should reports be accessible to others?

Perhaps we can establish a hyper-text format for the report and make it available over the Internet. Announcements of availability may be posted to a mailing list of all MOSIS educators.

C5. What does testing contribute to the designer's education?

In my experience, testing proved to be invaluable. I simply could not have replaced it with any currently available software tools that I am aware of. In my opinion, testing (and not simulation) process has the same educational value as systematic software testing and debugging would have in programming courses.

D. The MOSIS Community

D1. Funding is tight, and likely to remain so for the foreseeable future. What steps may be taken to maintain and enhance the educational values MOSIS provides to US technical strength?

As in any funded activities, accountability is important. Are chips used in some way to significantly enhance the learning of the students? If the answer to this question is positive and documentable, then funding may be justifiable. We also should seek ways to help instructors and institutions to further enhance the educational experience of students by using the fabricated chips. Sharing of test methodologies, tools and other instructional resources may be a good start.

D2. It may be possible to organize an electronic bulletin board for Educational MOSIS, along the lines of the MEMS Bulletin Board. This would be a chiefly student/student information sharing network. What actions would appropriate in this respect? How would such a network benefit the student and generate enthusiasm, better reporting and testing?

Excellent idea. Let's do it.

VLSI EDUCATION AND MOSIS - A CORNELL VIEWPOINT

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Cornell has used the MOSIS TinyChip service to introduce students to VLSI design of digital systems for about twelve years. ELE 439 "VLSI Digital System Design" is offered each Fall, and is taken by 40-50 students, including seniors, Masters-of-Engineering (1-year), and MS/PhD students. Typically about 60% co-register for ELE539 "Practicum in VLSI Design", which takes two semesters, and provides the experience of TinyChip design, fabrication, and test. Students are required to have a good background in digital logic and digital systems.

The course introduces students to the realization of digital devices and systems with full-custom CMOS. Designs are laid out with the aid of MAGIC, and simulated with IRSIM. At the outset the approach is "bottom-up", so that students become very familiar with MOS circuit behavior and analysis. Laboratory exercises allow students to appreciate the art of VLSI layout, the value of hierarchy, and the value of a good design style. The series includes a Built-in Logic Block Observer, which emphasizes the significance of incorporating test arrangements. In class we explore MOS structures which depart from CMOS, such as RAMs, dynamic logic, etc., with applications in arithmetic units, PLAs, etc.

Students who opt for just the first course work on a series of progressive exercises which culminate in a frequency counter for a noisy signal, which is laid out in MAGIC and simulated with IRSIM.

TinyChip projects are developed by groups of 3 students each, and follow a "top-down" approach. We set firm milestones for the proposal stage, functional simulation (in C or Galaxy), basic blocks (simulated with IRSIM), major blocks, and complete chip layout, with simulation. Clock driver designs are simulated with SPICE. Final layouts are reviewed by locally-developed well- and pad-checking software before submission to MOSIS. Designs typically comprise 4,000-5,000 transistors.

While fabrication is in progress, students learn about the way in which testing is carried out in industry, including both ASIC and production aspects. They use a PC-based tester for functional testing of a TTL ALU chip and an SRAM. This is followed by an introduction to high-speed testing with a Tektronix LV500 ASIC tester, and students test the ALU with this unit. On receiving the TinyChip sets from fabrication, the functional tester is used for overall evaluation. The ASIC tester allows the overall performance of the chip to be explored thoroughly, including "schmoo" plots with varying supply voltage, clock period, etc. The results are reviewed in terms of basic theory.

A1. Where is MOSIS used? Where should it be used?

In introducing students to the realities of MOS design and the potential of VLSI systems.

A2. What is the educational value of MOSIS for schools?

From an educational position, VLSI design is attractive for its combination of theory, analysis, practice, and measurement. By providing a target process and actual parts, MOSIS ties the whole framework together in a remarkably economical way. It is particularly useful as a "capstone design course" as defined by ABET, in view of its comrehensive nature.

It is important to note that industry does not usually provide this type of integrated experience, but recognizes its value.

B. Fabrication vs. Simulation

B1. What is the educational value of a completed design (hard chip)?

The combination of design, implementation, and testing is much more than the sum of the parts. Students become highly-motivated in exploring the limited space of a TinyChip, and in subsequently evaluating its performance. While in theory, the stresses and strains of TinyChip design and test could be introduced artificially, simulation cannot substitute adequately.

B2. Do we really need to fabricate chips for elementary classes?

Yes, provided that the chips will be tested and evaluated thoroughly.

B3. To what extent should virtual prototyping be used, especially in beginning classes?

Such classes should couple circuit extraction and simulation with layout, and so virtual prototyping is appropriate as designs are developed. In our experience, students who take the one-semester class gain from assembling a complete system this way. But there is a strong preference for the TinyChip route.

C. MOSIS in VLSI Education

C1. How does group size influence the educational value to the student of the MOSIS experience?

In our experience we find that groups of 3 seem to work well for projects of TinyChip size, and allow division of tasks in layout, simulation, test, etc.

C2. To what extent should the success rate of instructors' classes affect the priorities and funding of their subsequent classes?

It depends to some extent on how novel and/or complex the designs and circuit techniques are. A poor track record over a couple of years should be evident to NSF staff.

C3. What should the chip reports contain?

Clear evidence that chips have been tested thoroughly, and simulation results compared with measured performance. Ideally the reports should be evaluated in the educational institution concerned. It is important to distinguish the actual needs of the MOSIS service (essentially quality control) from those of NSF (educational value for money).

C4. How should reports be accessible to others?

Ideally yes, but in any case really interesting results are published in journals, etc.

C5. What does testing contribute to the designer's education?

It makes a designer more aware of the impact of test on the economics of production, and the need to anticipate test requirements at the design stage.

D. The MOSIS Community

D1. Funding is tight, and likely to remain so for the foreseeable future. What steps may be taken to maintain and enhance the educational values MOSIS provides to US technical strength?

(1) The basic argument is that, given access to high-technology, US students and recent graduates have demonstrated that they are outstanding at finding novel applications.

(2) Encourage instructors to develop prototype MOSIS chips which explore structures discussed in VLSI texts.

D2. It may be possible to organize an electronic bulletin board for Educational MOSIS, along the lines of the MEMS Bulletin Board. This would be a chiefly student/student information sharing network. What actions would be appropriate in this respect? How would such a network benefit the student and generate enthusiasm, better reporting and testing?

We have found it useful to operate a Web Home Page for our courses. The BB may be rather unwieldly.

Georgia Institute of Technology
Electrical and Computer Engineering
Martin A. Brooke

At Georgia Tech we are a little unusual since we are on a quarter system and the mixed signal community dominates in the number of faculty active in CMOS fab, classes, and research support. A lot of students go though a VLSI sequence taught by the computer engineering faculty. This has led to a slightly different structure to the use of MOSIS than other places. We have only a few core "VLSI" courses that teach digital system design, but, because of the quarter system, these typically do not provide time to do a really good job of fabricating designs in the class. We also have several analog oriented classes where students learn enough to make a fabrication project desirable, but once again the quarter system limits time in class to do a good job on fab. Thus we have created a system where students who commit to doing a fab in the eligible classes are required to take a no credit seminar course each quarter after the class to guide them through fabrication and testing of the chips. Our excellent record on testing and reporting on MOSIS projects is due to this structure.

When testing of chips in the class is required we have had TAs design chips beforehand and fabricate them in quantity sufficient for the class size expected. This has been used very well in a low noise CMOS design class where we wanted students to test real CMOS chips, and in a sub-threshold Carver Mead style class where the students used an ATE tester connected to the web to characterize prefabricated components in real time.

1. What tools and procedures are you using?

For analog:

Tools: Tanner Tools or
magic and HSPICE or
Cadence and HSPICE or
magic and PSPICE or
MDS

Procedures: Layout, extraction, and simulation or
schematic capture and LVS
are used to verify designs.
Test is usually done with SMUs for bias and Signal generators + scopes and analyzers

For digital:

Tools: MENTOR
Viewlogic

Procedures:
VHDL description is simulated first
Schematic capture and simulation of blocks next
then layout and LVS finally
Test is done on one of several digital testers available

2. Do you encourage the actual fabrication of designs for beginning classes?

Yes, but only if the students commit to attend the seminar class until the fab is complete and tested. We believe there is little value to fabrication if the chips are not well verified and tested by the students who designed them.

3. What experiences have you had in integrating research and education in your use of MOSIS?

These are tightly coupled in that many of the students who commit to finish a fabrication with MOSIS are taking an undergraduate research opportunity (UROP) sequence (three quarters) or are graduate students in the research program.

4. What suggestions for future services do you have that would enhance the interest in use of MOSIS?

For educational use the fast turnaround of designs would be the number one priority. If chips could be returned in 2-3 weeks (I know this is totally impractical in current fab facilities) we could get the whole experience in one class. I think the programmable logic devices provide this for digital design to a limited extent, but you cannot replace the fabrication experience for analog this way.

Maybe a gate array type of service would do the job. MOSIS could design a digital and an analog array and do rapid metal only fabs.

The 2 micron CMOS is fast becoming meaningless. It is so much easier to make things work in 2 micron than 0.5 micron or 0.35 micron that it may not prepare students for reality enough to do only 2 micron fab. Advanced classes should access advanced fab processes.

A. Role of VLSI and MOSIS in an Educational Setting

A1. Where is MOSIS used? Where should it be used?

MOSIS should be used when the time and resources are available to validate and test designs.

A2. What is the educational value of MOSIS for schools?

The US semiconductor industry owes it's success in part to students having a MOSIS experience. Due to MOSIS US companies have not had to train IC designers from scratch for so long that if the service vanished I'm not sure they would know what to do.

B. Fabrication vs. Simulation

B1. What is the educational value of a completed design (hard chip)?

For a student destined to an IC design career this experience is considered essential by most of the industry. The ability to get an A in a fabrication based class has much more meaning than in a simulation-only class. The ability take a chip design all the way to a functional part is not always correlated to high GPA and companies know it.

B2. Do we really need to fabricate chips for elementary classes?

I think some of the students in these classes should be able to do this. Many of the students can learn all they need doing programmable logic designs, or using off the shelf components. But for students who want to go into chip design careers the experience is essential.

B3. To what extent should virtual prototyping be used, especially in beginning classes?

This can provide all that some students need. But I do not believe a good simulation of real problems like cross talk or substrate coupling is practical for the classroom at present.

C. MOSIS in VLSI Education

C1. How does group size influence the educational value to the student of the MOSIS experience?

I think students working of different aspects of a team project is the best experience. Too fuzzy a team definition can lead to the "free loader" problem. But if each student’s part of the project is well defined and the overall grade is based on individual effort, quite large groups are practical. I believe a whole class can do one large project, if well planned.

C2. To what extent should the success rate of instructors' classes affect the priorities and funding of their subsequent classes?

This would be impossible to administer, at least at Georgia Tech. We share teaching assignments for many classes, and always the chips are tested some time after the class is over. It may be difficult to accurately identify the instigator of the success.

C3. What should the chip reports contain?

Some measured data. "The chip worked" is not a fair measure of the success of the project. Also a good fault analysis with corrective steps outlined should be considered a success.

C4. How should reports be accessible to others?

Maybe a WWW site of *magic* files and reports would be a good idea. Since the public pays for the fab, the results surely should be reported in the public domain

C5. What does testing contribute to the designer's education?

The most important part of the experience is testing. It is the completion of the task, and the only part which matters in the end. I never really believed in IC design until I saw the scope wiggle in a fashion at least a little like SPICE for the first time!

D. The MOSIS Community

D1. Funding is tight, and likely to remain so for the foreseeable future. What steps may be taken to maintain and enhance the educational values MOSIS provides to US technical strength?

Try to give fewer more extensive experiences. Maybe allow the only the top 10% of designs to be fabricated but in 0.8 um or 0.5 um CMOS. The cost would be similar, but the students most likely to actually use the skills will get a better experience. Realize that most VLSI designers come from at least the masters level. The advanced class program should be strengthened and the undergraduate program should be oriented more towards simulation.

D2. It may be possible to organize an electronic bulletin board for Educational MOSIS, along the lines of the MEMS Bulletin Board.

A WWW/ftp site with designs (mag files) and test results required to be posted would be great. This could become a national resource!

MOSIS Usage at the EE Department, University of Maryland, College Park March 21,1996

R. Newcomb and K. Nakajima

Preliminary Comments

Since VLSI circuits are key to today's high technology, it is the intent of the VLSI related faculty at the University of Maryland, College Park, to make available to all students of the EE Department the chance to design, simulate, fabricate, and test VLSI chips. In terms of courses, in the last three years this has involved a dozen faculty and over two dozen courses in which students can fabricate chips via MOSIS.

We encourage development in both the analog and the digital areas with the digital and analog activities primarily under the directions of Professors K. Nakajima and R. W. Newcomb, respectively. Although our students may participate in VLSI fabrications from the beginning junior-level electronics course on, emphasis is placed more at the senior and graduate levels. At the senior level we offer basic courses which cover the design at the transistor and gate level of both analog and digital circuits. These are followed by more specialized courses in both the analog and digital areas covering such topics as the design of neural networks and VLSI design automation.

1. What tools and procedures are you using?

1.a) **Analog**
1.a.1) **Primary simulation tool**: Spice, in several versions (Berkeley Spice on SUNs and PSpice on PCs)
1.a.2) **Primary layout tools**: MAGIC (on SUNs) and LEDIT (on PCs)
1.a.3) **Primary testing tools**: Analog measurement equipment in the Microelectronics Design Laboratory, including automated testing via PCs

1.b) **Digital**
1.b.1) **Primary simulation tool**: Spice, IRSIM, Mentor Graphics QuickVHDL
1.b.2) **Primary design/synthesis tools**: MAGIC, OCTTOOLS, PARTHENON, Mentor Graphics Autologic, PLDSynthesis.
1.b.3) **Primary testing tools**: Digital system testing equipment in the VLSI Design Automation Lab such as Tektronix DAS9200 Digital Analysis System, Hewlett-Packard HP82000/D100 IC Evaluation System, and Hewlett Packard HP1660A Logic Analyzers.

2. Do you encourage the actual fabrication of designs for beginning classes?

2.a) Analog: Definitely. We try to make fabrication of devices available to every student in our Department, beginning with the junior-level electronics course, ENEE 302 Analog Electronic Circuits

2.b) Digital: Definitely. Even for semicustom designs, their actual fabrication brings real-world engineering problems to the students -- meeting the deadline set by the third party is a good experience for them.

3. What experiences have you had in integrating research and education in your use of MOSIS?

3.a) Analog: This is one of the very positive aspects for our use at UMD. We are able to incorporate our research oriented undergraduates into VLSI as a primary research tool and more and more students are finding this is very advantageous for the job market.

3.b) Digital:
3.b.1) The use of MOSIS is a basis for our Combined Research and Curriculum Development activities at UMD. With the acquisition of a Hewlett-Packard HP82000/D100 IC Evaluation System through the recently awarded NSF CISE Research Instrumentation grant, our testing capability has been enhanced drastically.
3.b.2) New design concepts and methodologies as well as new architectures and algorithms are published in research papers. By actually implementing them, the students really understand how they work and also realize that many unexplained things need to be taken into consideration in the actual implementation.

4. **What suggestions for future services do you have that would enhance the interest in use of MOSIS?**

4.a) Analog:
4.a.1) Incorporation of several threshold levels, especially VTO=0, on one chip.
4.a.2) Make available "advertisement" literature for undergraduates about what students can do via MOSIS.
4.a.3) Make it easier to incorporate unfunded research student projects into the MOSIS funding.

4.b) Digital: Dissemination of good designs made in the past would motivate the students to challenge them.

A. Role of VLSI and MOSIS in an Educational Setting

A1. Where is MOSIS used?
4.A1.a) Analog: Primarily in our analog VLSI course, ENEE 493 VLSI Design (for design and layout), and related courses, such as ENEE 417 Microelectronics Design Laboratory (for measurements). However, we have a large number of classes in which fabrications are encouraged and are getting more and more faculty involved.

4.A1.b) Digital: Primarily in our digital system design courses such as, at the senior level, ENEE488Z "Computer-Aided Digital System Design Lab", and at the graduate level, ENEE644 "Computer-Aided Design of Digital Systems", ENEE 648T "VLSI Architecture", ENEE 748M "Advanced Digital Systems Design", and ENEE 748T "VLSI Design Automation".

A2. What is the educational value of MOSIS for schools?

4.A2.a) Analog: Immense. Our students feel they have accomplished something when they test a chip and it works. They also have an outstanding selling point on their resumes.

4.A2.b) Digital: Great. Introduction to real-world hands-on design experience, as well as a great opportunity to implement students' own ideas in chips without worrying about their failures as real-world products.

B. Fabrication vs. Simulation

B1. What is the educational value of a completed design (hard chip)?

4.B1.a) Analog: The thrill of having a completed chip in the students' hands is something that has to be seen to be believed. It enhances their commitment to engineering and gives them a real sense of worth.

4.B1.b) Digital: In a theory-oriented curriculum, like ours, making something real is extremely important for the students to understand the basics of engineering. By testing their chips, they also realize the importance of design for testability and the need to understand the fabrication and packaging processes.

B2. Do we really need to fabricate chips for elementary classes?

4.B2.a) Analog: In my opinion we should make fabrication available to our better students from the very beginning. It gives a sense of accomplishment which allows for deeper studies and more significant undertakings as the student advances.

4.B2.b) Digital: Yes, the students need to make something real. They learn a lot more when they test their chips.

B3. To what extent should virtual prototyping be used, especially in beginning classes?

4.B3.a) Analog: I am neutral on this and believe whatever an instructor can effectively use should be used.

4.B3.b) Digital: In my opinion, the students need to make something real.

C. MOSIS in VLSI Education

C1. How does group size influence the educational value to the student of the MOSIS experience?

4.C1.a) Analog: I believe that two is the optimum size for most educational groups since we need to give grades on an individual basis. I usually have the two working on slightly different aspects of the same circuit and find that way they can cooperate and enhance each other but each is responsible for their own work. With three or more I have not been able to have such effective learning.

4.C1.b) Digital: Two per project would be perfect. They work as a team and hence they need to communicate with each other. If more than two, various problems will arise such as scheduling of meetings.

C2. To what extent should the success rate of instructors' classes affect the priorities and funding of their subsequent classes?

4.C2.a) Analog: It should not unless a persistent problem shows up. Each class is different and these differences should be allowed and tolerated.

4.C2.b) Digital: It should not because the students must be responsible for design/testing and their failure will teach them a good lesson, too.

C3. What should the chip reports contain?
4.C3.a) Analog:
4.C3.a1) Date of measurement and signed professorial certification on validity of measurements
4.C3.a2) Otherwise, about what is presently requested, though including a listing of significant differences on any test transistors (which I would like to see on all student chips)

4.C3.b) Digital:
4.C3.b1) Date of measurement and signed professorial certification on validity of measurements
4.C3.b2) Testing method in addition to what is requested now.

C4. How should reports be accessible to others?

4.C4.a) Analog: I am neutral at present on this.

4.C4.b) Digital: If creative testing methods are used somewhere else, they are of great benefit to the students.

C5. What does testing contribute to the designer's education?

4.C5.a) Analog:
4.C5.a1) Confidence when it works and the need to consider and determine other factors when it does not.
4.C5.a2) Laboratory experience with generally non-cookbook laboratory work, something sorely needed by a number of electrical engineering students at all levels.

4.C5.b) Digital: The same as in the analog case.

D. The MOSIS Community

D1. Funding is tight, and likely to remain so for the foreseeable future. What steps may be taken to maintain and enhance the educational values MOSIS provides to US technical strength?

4.D1.a) Analog: As sometimes we do not use all of our allocations while at others we could use more, there may be some way to make midterm adjustments to allocations.

4.D1.b) Digital: The same as in the analog case.

D2. It may be possible to organize an electronic bulletin board for Educational MOSIS, along the lines of the MEMS Bulletin Board. This would be a chiefly student/student information sharing network. What actions would be appropriate in this respect? How would such a network benefit the student and generate enthusiasm, better reporting and testing?

4.D2.a) Analog: I think that the students may find this useful, but I myself do not want to be strapped by trying to keep up with it.

4.D2.b) Digital: In real-word design environment, know-how is very important. By exchanging their design/testing experience, the students will benefit a lot.

Department of Electrical and Computer Engineering
University of Massachusetts Dartmouth
Microsystems Design Laboratory
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The ECE department currently offers two undergraduate courses in microsystems design: an introductory course in digital VLSI design (ECE413) and an introductory course in analog VLSI design (ECE414), both of them at the senior level. Two graduate courses are offered when student interest warrants: ECE533 CMOS VLSI Design and ECE535 Analog CMOS VLSI Design. ECE413 is a required course for our Computer Engineering students, whereas ECE413 and ECE414 comprise a two semester sequence that is one of 6 required specializations in the ECE department. ECE414 (analog course) has as a prerequisite ECE413 (digital course). A unique aspect of ECE413 and ECE414 is their evolution into courses that have a significant telecommunications orientation, with digital signal processing, analog signal processing and high frequency RF topics covered.

The digital course (ECE413) utilizes time-honored CAD tools such as MAGIC, IRSIM, SPICE for student projects. The text used in by Pucknell and Eshragian and emphasizes CMOS digital design, with additional infomation provided to cover telecommunications topics. The students are required to do a design project as part of the course. These projects have as a minimum 250 transistors and must be clocked in some fashion. The students are also encouraged (but not required) to use their design project as part of their larger senior design project, which is supposed to take their entire senior year. Those students who want to incorporate their course project into their senior design project must have a substantial course design project, have a "fall back position" in case their fabricated IC doesn't work, and promise to file a full test report. In recent years, only those students incorporating their course design in their senior project have had their designs fabricated by MOSIS. In the past, we have had students design 4th order digital high pass and low pass filters, error detection and correction systems and microcontrollers. All of these systems are designed at the end of the student's first course in digital VLSI design.

The course ECE414 (analog) uses the text by Allen and Holberg, Analog CMOS Integrated Circuit Design. MAGIC and SPICE are used, although L-EDIT is being investigated for use in this course and ECE413. Students use not only the classic lecture-homework-test structure of this course, but they also do a series of design/layout laboratories ranging from current mirror design to switched capacitor network design using an operational amplifier (which the students also design, layout and simulate). Included in this course is the use of the "Analog Design Resource Kit" that provides a pre-fabricated chip set that includes circuits, covered in class and design problems, that the students can perform measurements on right after the material has been covered in class and in conjunction with design laboratories. The students have a final course project to do, which last year was the design, layout (and possible fabrication) of a tunable switched capacitor low pass filter circuit. The only designs fabricated are for those students returning to the university in September so that test reports can be submitted to MOSIS.

ECE 533 and ECE 535, the graduate microsystems courses, follow similar guidelines, with the exception that the analog text by Gray and Meyer is used and the students are required to do at least one term/research paper on a contemporary topic from the recent literature.

We have had sporadic research/education success with our undergraduates and their design projects. However, the few that we have had are quite successful. One recent project was the design, layout and fabrication/test of a complementary fully regulated cascode operational amplifier. This project, done by a senior student was not published to our knowledge and had 110 dB of gain, a GBW of 8 MHz and fast slew rates of nearly 10

volts/microsecond. This project came about by having the student use the design/layout as a means to test the layout/simulation tools when changing computer platforms and operating systems. Graduate level designs have included high speed flash analog-digital converters, DSP chips, and an analog IC used to model the human auditory system.

We have chosen to concentrate on full custom layout at UMass Dartmouth because of the increasing emphasis on analog, mixed, and high frequency telecommunications design in the laboratory. We have used automated place and route tools for digital work, but much of the low and high frequency analog work still requires hand drawn layouts for reduction of parasitics and special RF structures. In addition to the full custom layout tools mentioned above, we also use the EESof RF/microwave tools such as Libra, LineCalc, Touchstone, etc., for help in our HF designs. We also have a wire bonder for bonding dies onto HF microstrip for test.

A. Role of VLSI and MOSIS in an Educational Setting

A1. Where is MOSIS used?

In the senior year and for advanced educational and research projects

A2. What is the educational value of MOSIS for schools?

The value is very high, especially among our senior students. They have the capability to integrate their chip designs into their senior design projects, almost a requirement for some of the complex designs the students are working on. Of course, it is required for research.

B. Fabrication vs. Simulation

B1. What is the educational value of a completed design (hard chip)?

See above.

B2. Do we really need to fabricate chips for elementary classes?

Absolutely, although there is probably a good arguement for not making that the end goal. Rather, if the chip is being integrated into a more complex senior or graduate level design project, more educational value results since this mechanism provides a more real-life example of engineering in the workplace--designing ICs for a product rather than designing an IC just for the ICs sake

B3. To what extent should virtual prototyping be used, especially in beginning classes?

To a certain extent, this already goes on with probably half of my students who do not choose to go to fab with their designs. If the student's only desire is to have the class, virtual prototyping and the design experience it gives is still a desirable educational experience.

C. MOSIS in VLSI Education

C1. How does group size influence the educational value to the student of the MOSIS experience?

Groups of no more than 2. Anymore becomes unwieldy unless the project is very complex, and that really should only happen for advanced courses.

C2. To what extent should the success rate of instructors' classes affect the priorities and funding of their subsequent classes?

In most cases, the student project is the student's, not the faculty member's. While the faculty member provides oversight and advice, the faculty has to rely on the results presented by the student as the final measure before sending out to fab. Also, with more complex designs being attempted, it is inevitable that some designs will not work. Therefore, unless the faculty member has a track record of several years of all non-functional chips, the success rate should not be used as a metric for continued funding.

C3. What should the chip reports contain?

As much as possible, although that can be difficult with the current email report mechanism. Figures, etc., obviously are not possible using the current system. Although unweildy, mail in reports will contain much more information. I require students to submit a full report of both simulation and test, which could be forwarded to MOSIS/NSF.

C4. How should reports be accessible to others?

Possibly

C5. What does testing contribute to the designer's education?

A lot. Our students use the ICs in their senior projects, and so the motivation to produce working parts is very high. Testing further motivates them to learn new equipment (logic testers, logic analyzers, RF/HF equipment) on an IC that they have speced out.

D. The MOSIS Community

D1. Funding is tight, and likely to remain so for the foreseeable future. What steps may be taken to maintain and enhance the educational values MOSIS provides to US technical strength?

The current funding in our case is sufficient, as are the procedures in place. With the WEB in place, there might be mechanisms for shared experiences, WEB-based labs, etc., that could provide nearly identical experiences

D2. It may be possible to organize an electronic bulletin board for Educational MOSIS, along the lines of the MEMS Bulletin Board. This would be a chiefly student/student information sharing network. What actions would be appropriate in this respect? How would such a network benefit the student and generate enthusiasm, better reporting and testing?

It would give students a template or idea of what makes up a good report and give them ideas on what they should be thinking when going through the entire design process. Care must be taken, however, in identifying "excellent" reports that students can use as models.

The University of Michigan VLSI Program

Richard B. Brown

Tools

At Michigan, we have integrated a uniform set of commercial CAD tools into the undergraduate and graduate curriculum, as shown in the table below (first digit of the course number indicates year; e.g., EECS270 is a sophomore-level course, EECS317 is junior-level, etc.)

VLSI-related Courses (* Primary VLSI Sequence)	CAD Tools S	D	A	P	F	V	H	T	M	C
*EECS270, Intro. to Logic Design	S	X		X						
*EECS317, Semi. Dev. & Dig. Elect.	S			X						
EECS318, Analog Electronics	S	X								
EECS370, Intro. to Computer Org.	S	X								
EECS373, Des. of uProc. Systems	S	X								
EECS411, Microwave Circuits I	S									
EECS413, Monolithic Amp. Circuits	S			X						
EECS423, Solid-State Device Lab	S									
*EECS427, VLSI Design I	S	X	X			X	X	X		
EECS425, Integrated Circuits Lab.	S	X	X			X	X	X	X	
EECS470, Computer Architecture	S	X		X						
EECS522, Analog ICs	S	X		X	X					
EECS525, Solid-State u-Wave Circ.	S			X	X	X				
EECS527, CAD for VLSI	S			X		X				
EECS579, Digital System Testing	S	X		X						
*EECS627, VLSI Design II	S	X	X			X	X	X	X	X

S Schematic Capture	V Design Verification
D Digital Simulation	H Hardware Description Language
A Analog Simulation	T Testing / Fault Simulation
P PLD Tools	M Microwave Simulation / Optimization
F Full Custom Layout	C Silicon Compilation

For course work, we support the full Mentor Graphics tool suite, plus Verilog from Cadence, EEsof from HP for microwave design, and the EPOCH silicon compiler from Cascade Design Automation.

Use of a uniform, commercial toolset has brought a number of benefits:

- Encouraging proper engineering design methodology.
- Reducing the amount of time spent by faculty and students learning tools.
- Familiarizing students with full-function tools.
- Enabling interactions of many kinds with industry.

Graduate Kernel

A significant improvement in our graduate VLSI education was made in 1992, when we established a VLSI kernel (requirements for a focus of study) for M.S. and Ph.D. students. At Michigan, graduate students declare major and minor areas of study; the one exception to this is the VLSI area, which serves as both major and minor area because of the its breadth. The VLSI program straddles the boundary between EE and CS, providing the broad background needed by students to work effectively in integrated circuit design. Courses in the four areas covered are shown below:

VLSI Program Course Requirements

Area	Required Courses	Other Recommended Courses
VLSI	427, 522 or 523, 579, 627	411, 413, 511, 525, 534
Solid State	423 or 425	421, 422, 424, 425, 520, 521, 528, 540, 541
CAD/Software	426 or 527, 482 or 483	476, 481, 574, 575, 581, 582, 583, 586
Architecture	470	478, 570, 572, 577

Students must take a circuit fabrication course on one end of the spectrum, and compilers or operating systems on the other end. This program is an excellent fit for students working in our system-building research projects, and VLSI Program graduates have had an enthusiastic reception in industry.

VLSI

411 Microwave Circuits I
413 Monolithic Amplifier Circuits
427 VLSI Design I
511 Microwave Circuits II
522 Analog Integrated Circuits
523 Digital Integrated Circuits
524 FET and Microwave Monolithic IC Technology
525 Solid State Microwave Circuits
526 High Perf. Dynamic Device Models & Circuits
534 Des. and Char. of Microwave Devices and Monolithic Circuits
579 Digital System Testing
627 VLSI Design II

Solid State

421 Properties of Transistors
422 Semiconductor Materials
423 Solid-State Devices Laboratory
424 Integrated Circuit Process Technology and Process Integration

425 Integrated Circuits Laboratory
520 Theoretical Methods for Solid-State Electr.
521 High-Speed Transistors
528 Principles of Microelectronics Process Technology
540 Applied Quantum Mechanics I
541 Applied Quantum Mechanics II

CAD/Software

426 Fundamentals of Electronic Computer-Aided Design
482 Introduction to Operating Systems
483 Compiler Construction
476 Foundations of Computer Science
481 Software Engineering
527 Computer-Aided Design for VLSI System
574 Theoretical Computer Science I
575 Theoretical Computer Science II
581 Software Engineering Tools
582 Advanced Operating Systems
583 Programming Languages
586 Object-Oriented Databases

Architecture

470 Computer Architecture
478 Switching and Sequential Systems
570 Parallel Computer Architecture
577 Reliable Computing Systems

Keys to Success

Our introductory and advanced VLSI courses are project oriented. A major improvement in VLSI I (EECS427) was made when we redesigned its junior-level prerequisite course (EECS317) to have more of an integrated circuit (as opposed to terminal) orientation, included in it all of the transistor-level circuit material we had previously taught in the VLSI course, and required both EE and computer engineering students to have this prerequisite course. The result is that we can do significant projects in the semester-long introductory VLSI course.

We feel it is very important for students to design (one time) at the mask level. The introductory course is built around a baseline 16-bit microcontroller architecture which students modify to fit an application of their choice. They design their projects mostly full-custom, in groups of 3 to 5; the project is paced by assignments that are due each week.

In the advanced course, students use the EPOCH silicon compiler to implement their designs. Suggestions from the instructor, other faculty members, and industrial contacts help them to find applications close to their own interests. Many chips related to Ph.D. projects have been designed in this course. A typical project would be a special-purpose microprocessor having 250,000 to 1M transistors.

1. What tools and procedures are you using?
Primarily Mentor, Cadence, Synopsis, Cascade --- See above.

2. Do you encourage the actual fabrication of designs for beginning classes?
We make fabrication available to students whose projects are worthy, and who will test the chips. Fabrication is a big motivation for students, even though not everyone is able to take advantage of it.

3. What experiences have you had in integrating research and education in your use of MOSIS?
Many students at Michigan use MOSIS in their research projects, and, as mentioned above, many students design chips related to their graduate research in our VLSI courses.

4. What suggestions for future services do you have that would enhance the interest in use of MOSIS?
MOSIS should continue to gain access to aggressively scaled CMOS processes and to other interesting advanced semiconductor processes.

A. Role of VLSI and MOSIS in an Educational Setting

1. Where is MOSIS used? Where should it be used?
Michigan students fabricate chips designed in the VLSI courses and typically test them in the digital testing course (EECS579 -- an HP82000 D400/D200 is used for testing, with Summit software for converting test vectors to HP tester format.) In addition, graduate students use MOSIS to fabricate chips of larger integration levels than what are practical in our lab, and to verify functionality of the circuit design when the target process is being brought up in our own lab.

A2. What is the educational value of MOSIS for schools?
Testing is as important as any other aspect of VLSI. To complete the cycle, a student must have the circuit fabricated and spend time learning to test it. Ability to debug any kind of circuit is a valuable skill, but debugging prototype integrated circuits can be especially demanding --- there are too few engineers who are good at it.

B. Fabrication vs. Simulation

B1. What is the educational value of a completed design (hard chip)?
Simulation is a vital part of the process, but prototyping the real chip adds much to the educational experience.

B2. Do we really need to fabricate chips for elementary classes?
The projects we do in the introductory class are certainly of a size and complexity that merits fabrication. Students have felt so strongly about fabrication that they have negotiated leaves of absence with employers to test the chips.

B3. To what extent should virtual prototyping be used, especially in beginning classes?
At the circuit and layout level, we have extensive verification. In the beginning class, ISA-level verification is limited to focused testing.

C. MOSIS in VLSI Education

C1. How does group size influence the educational value to the student of the MOSIS experience?
Until this term, I have allowed no more than 3 students per group, but because of a large class size, I am allowing as many as 5 per team now. To my surprise, it is working well in 12 of 13 groups.

C2. To what extent should the success rate of instructors' classes affect the priorities and funding of their subsequent classes?
In most class projects, there is little excuse for circuits not being fully functional. I would be in favor of linking future funding to past success, if it could be implemented without a lot of trouble. There are disadvantages of doing so: people might not be so willing to experiment with new circuit techniques, and the veracity of reports might not be as good as it is now.

C3. What should the chip reports contain?
They should be short summaries. If they are longer, you will be sure nobody reads them.

C4. How should reports be accessible to others?
I doubt there is much need for anyone other than MOSIS personnel to read them.

C5. What does testing contribute to the designer's education?
Testing provides a great deal of satisfaction (motivation for future work) in the typical case. In cases wherein the chip does not function properly, important lessons are learned that will not be forgotten.

D. The MOSIS Community

D1. Funding is tight, and likely to remain so for the foreseeable future. What steps may be taken to maintain and enhance the educational values MOSIS provides to US technical strength?
Do not discontinue the support of class accounts. Allow universities to use the funds at MOSIS with some flexibility to serve their students/courses in the best way. There is much variation in curriculum structure, academic year organization, scheduling of courses, etc., which calls for flexibility.

D2. It may be possible to organize an electronic bulletin board for Educational MOSIS, along the lines of the MEMS Bulletin Board.
Just have everyone put their stuff on the web. See ours at:

http://www-personal.engin.umich.edu/~brown/Eecs427/
http://wwwpersonal.engin.umich.edu/~brown/Eecs627/
http://www.eecs.umich.edu/VLSI/

Microelectronics System Design
Department of Electrical and Systems Engineering)
Oakland University
Hoda S. Abdel-Aty-Zohdy

The Microelectronics Sytstem Design Lab (MSDL) has expertise, tools and facilities to build Application Specific Integrated Circuits, Integrated Signal Processing Circuitry, Sensors and Actuators Integrated Interfacing Circuits, Neural Networks analog and digital ICs for automotive electronics and other applications.The School of Engineering and Computer Science instructional programs emphasize systems engineering concepts which recognize the interdisciplinary nature of technological problems. Student designs are fabricated through the ARPA/NSF MOSIS facilities. The total design experience, from concept to tested physical prototype, is a must for computer engineering education.

VLSI Educational Experience at OU through MOSIS

Effective use of electronic design automation tools and accessible, reasoably priced circuit production facilites are the essential cornerstones for understanding and exploiting modern microelectronic systems. MSDL has the tools for devising microelectronic systems; these tools produce a digital file for circuit production. Simulation tools are used to accurately predict the performance of the specified design from the digital description alone. Although such simulation may be enough to ascertain certain behaviors, often an actual part must be made as a proof of the entire design. The following courses are offered (courses using MOSIS are in boldface):

CSE 171 Introduction to Logical Design and Microprocessors
EE 384 Electronic Materials and Devices
EE 378 Design of Digital Systems
EE 485 MOS VLSI, Semicustom Design of Digital ASICs
Tools: MAGIc, OCTOOL, IRSIM, OASIS
EE 487 Integrated Electronics
Tools: SUPREM, PISCES, SPICE, Tanner Tools
EE 495-CSE495 Special Topics
EE 490 Senior Project

EE 581 Integrated Circuits and Devices
Tools: MINIMOS, LEDIT, PISCES, SUPREM
EE 585 MOS VLSI Semicustom Design of Digital ASICs
Tools: Same as in EE 485
Text: Weste & Eshragian, "Principles of CMOS VLSI Design", 2nd. Ed.
References: Reinhard, "Introduction to Intregrated Circuits Engineering" (Chapter on MOS Integrated Circuits Fundamentals)
Neudeck, "Modular Series on Solid State Devices, vol. 2: The PN Junction Diode"
EE 683 Advanced MOS VLSI / Advanced Analog/Digital Systems Design
Tools: SPICE3, MAGIC, OCTOOLS, IRSIM, OASIS
Text: Ismail & Fiez "Analog VLSI Signal and Information Processing"
References: Allen & Holberg, "CMOS ANALOG CIRCUIT DESIGN"
Mead, "Analog VLSI and Neural Systems"
Weste & Eshragian, "Principles of CMOS VLSI Design", 2nd. Ed.

EE 595 Semicustom Design of ASICS using FPGAs
Tools: Viewlogic, Xilinx
EE 595 Special Topics
EE 690, EE 691, EE 795 Graduate Projects and Thesis

Comments about the various tools

OCTOOLS 5.2 suite

Full custom and semi-custom designs using Standard Linraries /MSU2-3/, PLAs and Gate Arrays

Pascal-like description for cell specification, good library of cells, layout tools (vem), logic, circuit and timing simulation (MUSA)

Automatic placement and internal routing can be controlled for optimized layout (padpole andWolfe)

Placement and routing to Pad Frame available; use limited to TinyChips

Scalable Cell Library for 3 um, 2 um and 1.2 um CMOS compatible with MAGIC CAD tools

Designed cells modifiable (PHYT)

Powerful printing and plotting options, including scale, rotate, color

CIF file not compatible with MOSIS standard format

Simulation: good practical logic simulator, parameter extractor for MAGIC, SPICE, and IRSIM

MAGIC

Good for full custom design, lacks built-in cell library

Manual placement of cells, routing through Net-Routing, which helps manual routing

Full custom design tool; but need additional simulation tools

Supports various simulation tools,has good parameter extractor

Good interface to RSIM, for interaction in logic and timing simulation

CIF standard format output

OASIS

Design system that uses LOGIC III description language

Provides mixed-level simulation, automatic layout generation, format verification for design functionality, automatic tool for testing and fault coverage at gate level

Placement and routing can be automatic, final placement and cell-frame routing are manual

Semicustom design tools: direct layout parts not easy to include in simulation

Scalable, extensible cell libraries

Flexible simulations (switch-level, gate-level, Register-transfer level, behavioral level) recognize

high-level functional desfcriptions and hardware description. Discrete event simulation, not convenient for analog designs.

Automatic test pattern generation

Usable for FPGAs XILINX ABEL, and HDL for FPGAs.

VIEWLOGIC

WORKVIEW: VIEWSIM, Simulator and Interface for FPGAs; VIEWDRAW LCA Schematic Editor; and XACT Design Implementation for XILINX FPGAs.
MAGIC: VLSI Design
IRSIM: Switch Level Simulator
PISCES-IIB and MINIMOS: Device Level Simulators
OASIS: Open Architecture Silicon Implementation Software

- Compiler and Logic Synthesizer
- Simulator and Verifier
- Automatic Test Pattern Generator
- Automatic Layout Generator

Projected needs for Microelectronic Systems Prototyping and Fabrication

The educational VLSI progams are evolving toward a mix of full-custom and semi-custom components AND hybrid analog-digital elements, facilities for Multi-Chip Modules, MEMS and Flat-Panel display technologies. For the next few years MCMs should be available at all levels of VLSI education.

MCMs: high performance VLSI systems.
- Current design support software: Mentor Graphics 'MCM Station', Cadence 'Allegro'
- Current CAD platform: Sun workstations
- Prototype Fabrication: MCM Interconnect Designer's access Service (MIDAS)
- Substrate Technologies:
  - MCM-L
    - Cheapest
    - Wire bonding
    - Low Interconnect density
    - High thermal expansion coefficient
  - MCM-C (Thick film multilayer)
    - multi-layer possible with variety of dielectric pastes.
    - few problems with excessive shrinkage
    - manufacture entails series of firing steps
  - MCM-C (High temperature co-fired ceramic)
    - Similar to thick film multilayer, good for many layers
    - limited to refractory elements
  - MCM-C (Low temperature cofired ceramic)
    - Compatible with high-conductivity metals
    - Very low thermnal conductivity
  - MCM-D
    - high densities, fine lines
    - may be suitable for high frequency operations

MCM Workstations
- LIBRARIAN
  - Graphics Editor for geometric parts
- PACKAGE
  - Interactive and atomatic packaging of logic to physical parts
  - Incremental schematic packaging
  - Forward annotate schematic-driven rules and constraints
  - Approximate real estate estimates
- LAYOUT
  - Placement and routing environment
  - Parameter ectractor for interconnect coupling
  - Multi-conductor crosslake and transmission line simulator
- Auto Therm
  - Thermal finete element analysis
  - All heat-transfer modes
- FabLink
  - Drafting and detailing
  - CAM outputs
- Hybrid Option
  - generation of printed resistors, terminators

DESIGN IN EDUCATION AND RESEARCH

Paul Hulina
Pennsylvania State University

The Computer Science and Engineering and Electrical Engineering Departments at Penn State offer a series of courses and provide resources for design exposure at varying levels for the education and research communities.

In the **VLSI area**, two courses are available at the junior/senior and graduate level.

CSE 477 - VLSI Digital Circuits provides exposure to integrated circuit device design, layout, masking, simulation and fabrication along with VLSI design techniques, system architecture and CAD design.

CSE 577 - VLSI System Design promotes engineering design of large-scale integrated circuits, systems and applications along with a study of advanced design techniques, architectures and CAD methodologies.

These two courses employ MAGIC and OCTOOLS for full custom and standard cell design along with IRSIM, BERKLEY SPICE and H-SPICE for simulation. The tools run on SUN workstations and little is available at the PC level. Testing is done with a Tektronix Digital Analysis System (DAS9100) containing pattern generator, data acquisition and trigger/timebase boards.

In the first course, students may choose to design using full custom or standard cell or a combination of the two. In order to submit a design for fab the associated students must sign up for a special topics course the following semester in order to insure adequate testing.

In **the rapid prototyping area**, two course are available at the junior/senior level.

CSE 412 - Embedded Processor Design provides prototyping of digital systems using microprocessors as the primary control mechanism along with programmable logic devices for special function implementation.

EE 497P - Rapid System Prototyping provides exposure to the tools and technologies needed to rapidly design and implement digital systems.

These two courses employ PCAD and the CADENCE suite of tools running on a number of SUN
workstation located throughout the College, along with extensive XILINX development resources.

The College of Engineering provides physical resources and a staff that is part of the Center for Electronic Design, Communication and Computing. The Center functions as a focal point in supplying expertise and aid in design and prototyping for the educational and research communities within and external to the University. The Center hosts a number of CAD tools including CADENCE, PCAD, AUTOCAD, IDEADS on several SUN 20 dual procesor machines along with a number of SUN Sparc 5's.

A. Role of VLSI and MOSIS in an Educational Setting

A1. Where is MOSIS used? Where should it be used?

MOSIS has been used to support the fabrication of chips for beginning and advanced education as well as for research. MOSIS is still very cost effective for TinyChip fabrication and is best suited in this role. It appears that other places (such As TSM in Taiwan) provide more aggressive technologies at a lower cost than can be provided by MOSIS. MOSIS can still be beneficial in the research area by using the TinyChip service to fab several small parts of the system for verification before committing the complete design to fab.

A2. What is the educational value of MOSIS for schools?

It provides a vehicle whereby students can get valuable exposure real world issues in the design cycle and provides a more marketable product for the universities.

B. Fabrication vs. Simulation

B1. What is the educational value of a completed design (hard chip)?

Actually designing and getting hardware (chip) to function as specified is a rewarding experience for students and provides tremendous motivation. However, this experience can also be achieved via an FPGA based design and implementation.

B2. Do we really need to fabricate chips for elementary classes?

Recent figures indicate that roughly two thirds of commercial designs are prototyped prior to a final chip design. Very few companies are actually doing custom design. We need to look at what industry is doing and what skills and training they need from their engineers.

B3. To what extent should virtual prototyping be used, especially in beginning classes?

Simulation is a valuable tool and students should be exposed to it early in their study so that they become comfortable with the use of design tools. However, we must guard against giving students the impression that the simulation can solve all their design problems. They must have exposure to the hardware side and all its problems at the junior/senior level.

C. MOSIS in VLSI Education

C1. How does group size influence the educational value to the student of the MOSIS experience?

To some extent, it is influenced by the size of the project. In general, an ideal group is two but in some instances a larger group size may be beneficial. The objective is to insure that the individuals are not overwhelmed by the design task.

C2. To what extent should the success rate of instructors' classes affect the priorities and funding of their subsequent classes?

The desire to hold someone accountable is a noble one but somewhat unrealistic where many individuals are involved. At Penn State we have faculty at branch locations who share the class account and this makes a single point of contact accountability model very difficult.

C3. What should the chip reports contain?

Summary of test procedure and results. Important to benchmark against original design specifications.

C4. How should reports be accessible to others?
Via a bulletin board (as in D2) or WWW forum. Its important to share an overall description of the design and problems that were encountered in the various phases of the project.

C5. What does testing contribute to the designer's education?

Makes the student aware of the potential problems associated with a design, and testing procedures that can be employed. Finally, the student gains some appreciation for the design for testability concept.

D. The MOSIS Community

D1. Funding is tight, and likely to remain so for the foreseeable future. What steps may be taken to maintain and enhance the educational values MOSIS provides to US technical strength?

If funding must remain level or be curtailed, then the most cost effective use of the MOSIS structure in the fabrication of TinyChips. With this scenario, the most students get the needed exposure.

D2. It may be possible to organize an electronic bulletin board for Educational MOSIS, along the lines of the MEMS Bulletin Board. This would be a student/student information sharing network. What actions would be appropriate in this respect? How would such a network benefit the student and generate enthusiasm, better reporting and testing?

It would be great if students could post high level descriptions of their designs and elaborate on design and testing problems and pitfalls that they encountered.

VLSI Design Issues for the Future

Joseph Cavallaro
Department of Electrical and Computer Engineering
Rice University

At Rice University, an introductory VLSI design course that uses the MOSIS Service for fabrication has been operating for more than ten years. For the past eight years while I have been at Rice, the course has concentrated on the design of digital microcontrollers implemented in CMOS. The MOSIS experience is very important to the students and provides much of the motivation for the course. The concept that a unique project can be designed and fabricated in an academic year is very exciting to the students. The design, simulation, re-design, and final chip testing process builds important team design skills sought by industry. The students give class presentations at the end of each term and are required to report on the success of the chip to the entire class. This instills a sense of responsibility concerning the design. Many companies are impressed with students who have taken a VLSI course where the design is actually fabricated and tested. The course is reported to help students secure a good job at a good company.

As the state of the art in industrial VLSI design is moving at such a rapid pace, it may be time to evaluate the goals of introductory VLSI courses. Ten years ago, educational and research chips designed in universities were similar to some industrial efforts. These days, the speed and density achievable in commercial products is increasing at an amazing rate. It would be useful to investigate the possibility of migration to a more advanced MOSIS technology for introductory courses. The commonly used academic design tools are mature but may benefit from some updating for the newest computer hardware and operating systems. Although there are a number of fine textbooks on VLSI Design, a workbook of MOSIS TinyChip case studies oriented toward the design methodology with the common academic design tools would be beneficial. At Rice, there is excellent local interaction with Texas Instruments. Tours of a working fab line are arranged from time to time for the semiconductor device and VLSI courses. Perhaps, greater interaction and support from industry or groups, such as SEMATECH and SRC, for introductory VLSI education would help to supplement the experience for students. Although the following discussion will focus on experience with digital system design, Analog VLSI, Multi-Chip Modules, and Micro-Electro-Mechanical Systems are also important areas for MOSIS support.

Currently at Rice, the MAGIC, SPICE, AND IRSIM tools are used for the introductory VLSI course, Elec 422. The students are encouraged to build complex microcontrollers and the Berkeley PLA tools, including MEG and MPLA are used for finite state machine design. Each group of two or three students in a class of roughly twenty-five seniors and graduate students proposes an idea for a TinyChip project at the beginning of the fall semester. We spend the first few weeks of the semester in a design refinement process with the students. Each project typically contains an 8-bit data path controlled by a PLA implementing a finite state machine with around 16 to 64 states. A variety of projects have been built ranging from games and vending machine controllers, to cache controllers, simple RISC processors, simple DES encryption chips, and arithmetic units such as division, square root, and CORDIC.

The spring semester continuation VLSI course, Elec 423, stresses testing methodologies. Until the chips arrive in late February, various testing strategies and interfaces such as test access port (TAP) are discussed. Automatic test generation software, such as the test generation system (TGS) from USC, is presented and used to test combinational logic examples. In order to test the MOSIS fabricated chips, the PC-based Omnilab test system

from Orion Instruments, a small California company, is used. Conversion software takes the IRSIM test vectors used to simulate the design and converts them into the Omnilab binary format. This interface software has been developed at Rice and thus with moderately low-cost equipment, the chips can be tested at up to about 17 MHZ. After the chips are thoroughly tested, there is a laboratory session where the fabricated chips are observed and photographed through a microscope. The observation of their fabricated design through a microscope strengthens the understanding of many of the processing issues for the students.

For the last three years, an advanced digital VLSI course, Elec 522, has been offered at Rice. This year, MOSIS support for the advanced course has begun. In the advanced class, Octtools, Lager, and Hyper are used, along with an introduction to Ptolemy to give students a high level design experience. The introductory VLSI course is a prerequisite and there are many contrasts between custom design and place and route systems that are discussed. Both VLSI courses integrate with the computer architecture and DSP courses at Rice. The VLSI courses also integrate with the semiconductor curriculum where students are more concerned with transistor, processing, and manufacturability issues.

MOSIS fabrication has also been used for various research projects. Through a supplement to an NSF RIA grant, a number of custom chips for a prototype systolic array for the computation of the singular value decomposition (SVD) of a matrix were fabricated. This array used 16-bit co-ordinate rotation (CORDIC) arithmetic units to perform the inverse tangent and sine/cosine transformations needed for Givens rotations used in the SVD problem. Initially, TinyChips were designed in MAGIC to verify the behavior of the functional units. These designs were later integrated with Octtools and Lager. The commercial Powerview package was also used to help with some of the chip simulations and to provide array simulation and output for printed circuit board design. The resulting chip was a large design packaged in an 84 pin PGA. It was successfully fabricated in 2.0 micron CMOS. Prototype PCB's to interconnect an array of sixteen of these chips were also designed and fabricated.

In terms of the design tools, the academic tools have been preferred, because of the open architecture, and the MOSIS support. However, some of the software packages could benefit from updating. For some time, the staff at MOSIS has provided support for the MAGIC technology file. However, related tools such as the Berkeley PLA tools (MEG, ESPRESSO, EQNTOTT, AND MPLA) are less of a priority. Although various groups have provided support for the tools through the years, there tends to be the need for local maintenance at each site. It may be useful to continue to improve the coordination and distribution of support information. Testing equipment can also a problem due to cost and complexity. At Rice, the semi-customized Orion Omnilab test equipment gives the students a testing experience which is similar to using the IRSIM simulator. However, since this equipment will need to be replaced in the next few years, it will be difficult to locate a similar low-cost "logic analyzer" system. The variety of test equipment used at different universities also complicates the testing phase of the MOSIS experience for the students.

This year, the students have begun to build WWW homepages for each of the VLSI design projects. They have been internal to Rice University at this point, but there are plans to make the project homepages more widely available. Currently, the homepage gives a functional description of the project design. As testing is completed this spring, the students will add the testing results to the homepage.

A. Role of VLSI and MOSIS in an Educational Setting

A1. Where is MOSIS used? Where should it be used?

At Rice, MOSIS fabrication is used in introductory Elec 422, VLSI Design I and Elec 423, VLSI Design II, and in Elec 522, Advanced VLSI Design. It is very useful in both the introductory and advanced classes to provide students with a practical goal.

A2. What is the educational value of MOSIS for schools?

Chip fabrication through MOSIS is an integral part of the VLSI course. It is an important design experience for the seniors and graduate students.

B. Fabrication vs. Simulation

B1. What is the educational value of a completed design?

A completed design provides a proof of concept. Many of the design trade-offs required to complete a TinyChip enhance the learning experience. The physical I/O pin limitations of the TinyChip padframe require careful planning of the data bus and the resulting data path precision. Also, layout compaction and routing become important issues when completing the design. Without the real constraints of preparing for actual MOSIS fabrication, it is more difficult to motivate these important design issues.

B2. Do we really need to fabricate chips for elementary classes?

It is important to fabricate chips in the elementary VLSI classes. Preparation for fabrication forces a greater level of thoroughness in design rule checking, simulation, and design refinement. The students and instructors are aware that NSF and ARPA are investing substantial money in their designs. This leads to a greater level of responsibility.

B3. To what extent should virtual prototyping be used, especially in beginning classes?

A form of virtual prototyping is already done in the first Digital Logic course, Elec 326. This course at Rice uses Powerview for the laboratory exercises. Elec 326 is a prerequisite for the Elec 422 VLSI Design course.

C. MOSIS in VLSI Education

C1. Group size influence on the educational value:

Student groups of two or three students work well. In most groups, there are three students. This group size allows a somewhat more aggressive project, and also forces students to develop team interaction skills. VLSI design can be a very intense process, and the third person allows for more flexible task partitioning.

C2. Success rate of instructors' classes affecting priorities . . .

This can be a difficult issue, since there are many factors that influence the success of the fabricated chip. It may take some experimentation to determine and maintain the proper balance of project complexity and student skills. Further resources for instructors, especially junior faculty, should be developed.

C3. What should the chip reports contain?

The chip reports should contain a summary of the testing results. The report submitted to MOSIS may be a subset of the complete testing report prepared for the class. The chip report should describe whether the chip was functional, and the number of functional parts. If there was a problem with the chip, the students should try to locate the source of the problem in the design. An attempt should be made to report the maximum speed at which the chip was fully functional. In the complete class report, the test vectors used should be carefully described. The IRSIM simulations should be compared with the results of the chip testing, and the various waveforms compared.

C4. How should reports be accessible to others?

Within the course, the reports are typically presented at the last class of the semester. A summary is then sent to MOSIS. The summary reports can be made available through a WWW homepage for the class. As WWW technology improves, it will become possible to present graphically more of the raw testing results. The WWW pages can then be linked to MOSIS or to the NSF to bring together the experience at classes at the different universities.

C5. What does testing contribute to the designer's education?

Testing is crucial to verify the design process. If the design is carefully developed and thoroughly simulated, then in most cases, the testing should be straightforward. The testing should be as exhaustive as possible to uncover any possible flaws. In the testing phase, students realize the importance of the design for testability features hopefully incorporated in their design. Since they can no longer randomly watch additional internal nodes in the fabricated chips, the value of bringing out internal test signals, such as PLA controller state information, is better understood.

D. The MOSIS Community

D1. Funding is tight, and likely to remain so for the foreseeable future. What steps may be taken to maintain and enhance the educational values MOSIS provides to US technical strength?

Mosis funding is very valuable for teaching and research in VLSI design. Perhaps greater awareness of the valuable role that MOSIS provides in training engineers will encourage industry to contribute resources to supplement MOSIS.

D2. It may be possible to organize an electronic bulletin board for Educational MOSIS, along the lines of the MEMS Bulletin Board. This would be a chiefly student/student information sharing network. What actions would be appropriate in this respect? How would such a network benefit the student and generate enthusiasm, better reporting and testing?

As mentioned above, WWW homepages for each of the student design projects are very useful. This can help to convey the goals of the design, and results of the project to others. These pages can be organized at the various universities and then linked together so that the wide spectrum of courses can be visible.

Stanford University
Mark Horowitz

Stanford has either a modest program in VLSI or a large one, depending on what you consider VLSI. The core sequence in only 3-4 classes: Intro to VLSI, VLSI Project Class (part A, B, where B is testing), and Adv VLSI Design. In addition to these core classes, there are a large number of other IC design classes ranging from analog design to DSP. For this note I will try to incorporate the full range of classes, but I know the VLSI core best, since these are the classes that I teach each year.

A listing of the classes and description is included at the end if you are interested. Here are simply the class names:

218. Semi-Custom VLSI Systems
271. Introduction To VLSI Systems
272A. Design Projects In VLSI Systems
272B. Testing And Simulation Of VLSI Systems
313. Digital MOS Integrated Circuits
314. RF Circuit Design
315. Analog MOS Integrated Circuits
318. Computer-Aided Design Of VLSI Systems
371. Advanced VLSI Circuit Design
377. Computer-Aided Analysis Of VLSI Systems
487. Digital Signal Processing Architecture And Systems

One point that is often overlooked is that at a university there is a lot of education that happens outside of a class room. Most of the faculty spend a considerable amount of time working with students. While one hopes this ultimately will help the research program, a large part of this exchange is really educating the student in state-of-the-art techniques. And it is often in these situations where MOSIS is critical.

1. What tools and procedures are you using?

218 Semi-Custom VLSI design

Viewlogic schematic entry; Actel / Xilinx

Students in this class learn about logic design issues and tools for semicustom design. The final project is something that fits in an Actel part, on a predefined board that fits in a PC.

271 Introduction to VLSI Design

Magic; irsim; verilog; vcheck (a 2-phase clocking check); synopsys; snoopgen (creates irsim vectors from verilog)

This is a large lecture class (100-150 students) where the students work on homework assignments to learn the tools. Since the students learn four tools in about 4 weeks, the assignment are pretty specific, and much of the information that is needed is given in the assignments. The final project of the class takes about 3-4 weeks, and students working in groups of 2 design the datapath of an 8bit processor, create the layout, and then use irsim to check its functionality. This is a paper design project. Note: we don't use SPICE in this class. To ensure that the groups complete the project, the teaching staff meets with each group during the project. During the last quarter only 2 groups out of 60 did not complete the project.

272A Design Projects In VLSI Systems
Magic; irsim; verilog; vcheck (a 2-phase clocking check); magellan; synopsys; lager (for timberwolf); snoopgen (creates irsim vectors from verilog)

This is a project class. Students working in groups of 2 choose a chip design, code it in verilog, debug it, synthesize the control and do a custom datapath layout. The chips are then checked with irsim to make sure that they work and then are shipped to MOSIS. The class projects are TinyChips, either 2u or 1.2u

272B. Testing And Simulation Of VLSI Systems
irsim; MacTester; Testarossa Tester

In this class we talk about testing issues. First we run a fault simulator based on irsim to find out the fault coverage of the test vectors, and then talk about methods to increase coverage. We also have programs that convert irsim testfile to run the testers.

313 Digital MOS Integrated Circuits
314 RF Circuit Design
315 Analog MOS Integrated Circuits
371 Advanced VLSI Circuit Design
HSPICE; sue (a schematic editor, waveform viewer)

These are various 'circuit' classes at Stanford, and work on both analog and digital circuit design. They mostly use HSPICE, and 371 also uses Verilog.

487. Digital Signal Processing Architecture And Systems
Mentor DSPstation

This class is an advanced DSP class where students design complete signal processing chip. The chips are not sent for fabrication.

2. Do you encourage the actual fabrication of designs for beginning classes?

No. The first class only does a computer design. There are 150 people in this class.

3. What experiences have you had in integrating research and education in your use of MOSIS?

I think this is the critical issue that is often missed. Almost all of the students doing research that uses VLSI have taken the VLSI project class where they first learned how to use the tools. The process also works in reverse, since it is the advanced graduate students who learn how to use new tools and write the documentation/ homeworks for the classes.

4. What suggestions for future services do you have that would enhance the interest in use of MOSIS?

I think the main limitation in MOSIS usage is really money for chips. If more money were available, more people would submit chips.

What additional services should be provided depends on what we are trying to support. If we are trying to support system designers a 'LSI' like service would be nice. But I am not sure how this fits into education

A. Role of VLSI and MOSIS in an Educational Setting

A1. Where is MOSIS used? Where should it be used?

MOSIS is used for two purposes at Stanford. One is for the VLSI project class, and the other is for students to explore more advanced ideas that might be related to their research, but not directly part of it. I think this is where it should be used. If students will not test the chips, there is no point in fabricating them

A2. What is the educational value of MOSIS for schools?

I think the fact that the students are building a chips is an enormous motivational factor. The students in the project class spend about 150-200 hours on the project in an eight week period, much of it during the last 4 weeks. I don't think they would work so hard if there was not a chip attached. Dealing with a real chip makes many constraints seem more real (the die is a fixed size, and there is a fab deadline). But I am not sure about the realism factor. Since I constrain the designs to fit a specific style, nearly all the chips work (95+% work). So they don't get a feeling for debug

B. Fabrication vs. Simulation

B1. What is the educational value of a completed design (hard chip)?

See A2. I think it is really motivation, not realism

B2. Do we really need to fabricate chips for elementary classes?

No. I think the point of having fabrication in the first class does not make sense. Their projects will not be that interesting, and probably needs to be set by the teacher. For the project class $500 seems like a small investment for the 200 hours of student work.

B3. To what extent should virtual prototyping be used, especially in beginning classes?

In the introductory class, we have a fairly complete set of test that the designs need to pass -- the tapeout test for the follow-on project class. I think these are sufficient to work out the bugs in students designs. And there are enough of these type of bugs to keep the students busy.

C. MOSIS in VLSI Education

C1. How does group size influence the educational value to the student of the MOSIS experience?

Two people per team is the right balance between having some help and communication costs. In larger teams usually someone is just hanging on.

C2. To what extent should the success rate of instructors' classes effect the priorities and funding of their subsequent classes?

For standard digital design there is no excuse for chips not working. The tools are good enough that if a chip passes simulation it should work. For analog chips, the situation is a little different, but I still think the success rate should be high. The only chips that might have a higher failure rate are chips that use experimental circuits.

C3. What should the chip reports contain?

This depends on who is going to use them. My feeling is that noone looks at the MOSIS testing reports, so they are very short. Internally each student writes a fairly complete report that I keep to show next years' students to see what is possible. We are moving to put the chip documentation on the web.

C4. How should reports be accessible to others?

Just put it on the web. If someone is interested, they will find it.

C5. What does testing contribute to the designer's education?

Prove that the chip really works. What I really like is when the student takes the chip and uses it in a system. They the chips really get tested, and most of them have some additional features. But these are not found in the tester.

D. The MOSIS Community

D1. Funding is tight, and likely to remain so for the foreseeable future. What steps may be taken to maintain and enhance the educational values MOSIS provides to US technical strength?

I think the key is accountability. I think that when the chips are free many people submit chips that might not be well thought out. We need to have some standards so people think about what they submit for fabrication. I would like to have some money available for interesting projects, that enable students to do really creative stuff.

D2. It may be possible to organize an electronic bulletin board for Educational MOSIS, along the lines of the MEMS Bulletin Board. . .

I think this is not a good idea, since it takes someone to organize it. We could try to put stuff up on the web, and see what happens.

Stanford University

Here is a listing of the classes (from the catalog)

218. Semi-Custom VLSI Systems

Introduction to the design, architectures, and design automation of semi-custom integrated circuits. Hands-on experience in designing and prototyping a board level system using semi-custom VLSI. Topics: semi-custom design methodology; macro library, design entry and synthesis, simulation, automated placement and routing, and testing; performance optimization for macro library-based design; packaging; architectures of sea of gates, programmable logic arrays, and FPGAs. Prerequisites: basic knowledge of digital systems, logic design at the level of 182 and CMOS circuits at the level of 112, or consent of instructor.

3 units, not given 1995-96

271. Introduction To VLSI Systems

For Electrical Engineering, Computer Science, and Computer Systems Engineering students with background in computers, processors, and circuits. Large scale MOS design. Topics: MOS transistors, static and dynamic MOS gates, stick diagrams, programmable logic array design, MOS circuit fabrication, design rules, resistance and capacitance extraction, power and delay estimates, scaling, MOS combinational and sequential logic design, registers and clocking schemes, memory, data-path and control unit design. Elements of computer-aided circuit analysis and layout techniques. Prerequisites: 112; familiarity with circuits, logic, and digital systems.

3 units, Aut (Horowitz) TTh 2:45-4 Spr (DeMicheli) MW 11-12:15

272A. Design Projects In VLSI Systems

For students with research and applications interest in VLSI systems. Working in teams of two, students complete modest-sized CMOS chip of their own design. Project includes writing a functional model (in Verilog), using synthesis tools, custom layout, and simulation. Overview of the issues involved in VLSI design. Topics: design tools and techniques, complexity management, clocking issues, layout and floorplanning, design of large array structures, testing and testability issues. Prerequisites: 271, experience with digital design.

4 units, Win (Horowitz) TTh 1:15-2:30 lab by arrangement

272B. Testing And Simulation Of VLSI Systems

Continuation of 272A, simulating, testing, and elaborating projects designed in 272A. Students functionally simulate and test projects and report the results. Additional credit for more extensive work by arrangement. Lectures include simulation and testing techniques used in the lab. Prerequisite: completing the 272A design project.

2 units, Spr (Horowitz) TTh 9:30-10:45 lab by arrangement

313. Digital MOS Integrated Circuits

Analysis and design of digital MOS integrated circuits. Device and circuit modeling considerations. Circuit performance evaluation by means of simple approximations and computer-aided circuit analysis. Transistor-level design techniques for implementing specific digital circuit functions. Logic and memory subsystem considerations. Adjunct to courses in VLSI architecture and layout. Prerequisite: 112 or equivalent.

3 units, Win (Wooley) MWF 10

314. RF Circuit Design

Design of RF circuits for communications systems. Topics: the design of low-noise amplifiers at RF, passive and active filters, mixers, modulators and demodulators; review of classical control concepts necessary for oscillator design including PLLs and PLL-based frequency synthesizers. Design of high-efficiency (e.g., class E, F) RF power amplifiers, coupling networks. Behavior and modeling of passive and active components at RF. Prerequisite: 214.

3 units, Win (Lee) MWF 2:15

315. Analog MOS Integrated Circuits

Fundamentals of analog MOS integrated circuit design. Small-signal device and circuit models. Design of amplifiers, analog switches, sample and hold circuits, comparators, and voltage references. Analog subsystems, including A/D and D/A converters and switched capacitor filters. Prerequisite: 271 or 313.

3 units, Spr (Wooley) TTh 11-12:15

318. Computer-Aided Design Of VLSI Systems

Computer-aided synthesis of digital circuits. Analysis and design of exact and heuristic algorithms and description of current CAD tools. Topics: hardware modeling and modeling languages (e.g., VHDL, Verilog); architectural synthesis and optimization methods: (scheduling, binding, data-path and control synthesis), logic synthesis and optimization for two-level and multiple-level combinational and sequential circuits; library binding. Recommended: familiarity with logic design, algorithm development, and programming.

3 units, Win (DeMicheli) MW 3:15-4:30

371. Advanced VLSI Circuit Design

Overview of important issues in high performance digital VLSI design. Focus is from a system perspective (a fast processor, DSP, etc.), CMOS, bipolar (ECL like) and BiCMOS circuits. Topics: wire modeling, logic families, latch design and clocking issues, clock distribution, RAMs, ALUs, I/O and I/O noise issues. Final project involves the design of a subsystem for a high-speed processor. Extensive use of SPICE. Prerequisites: 271, 313 or consent of instructor. Recommended: knowledge of C and C-shells.

3 units, not given 1995-96

377. Computer-Aided Analysis Of VLSI Systems

Introduction to simulation techniques used in VLSI circuit and system design. Topics: formulation of circuit equations, modified nodal analysis, Gaussian elimination and LU decomposition, sparse matrix techniques, DC analysis of nonlinear circuits: linear multistep integration, relaxation based methods: Gauss-Seidel-Newton methods and waveform relaxation, timing verification and Penfield-Rubinstein technique, switch level simulation, event-scheduling and selective trace, functional level simulation, mixed-mode and heterogeneous simulation, distributed event-driven simulation, and hardware simulation accelerators. Prerequisites: 101, linear algebra (Math. 113).

3 units, alternate years, given 1996-97

487. Digital Signal Processing Architecture And Systems

The design and implementation of signal processing systems. Survey of a variety of architectures and the tools available to automate this task. Case studies in data communications and image processing. Topics: behavioral specification and hardware simulation of signal processing systems, hardware generation using silicon compilers, dedicated architectures, programmable architectures, real-time operating systems, array processors, architecture design tools, asynchronous design, and low-power implementation. Prerequisites: 271, basic DSP concepts, C Programming language, and UNIX.

3 units, not given 1995-96

University of Tennessee at Knoxville
Don Bouldin bouldin@utk.edu

1. What tools and procedures are you using?

Introductory Custom Design (ECE 651):

MAGIC
small custom digital cells
2 persons/project
MOSIS TinyChip fab

Introductory Semicustom Design (ECE 551):

Viewlogic synthesis
Xilinx P&R
2 persons/project
Xilinx 4005 Prototyping Board

Advanced ASIC Design (ECE 552):

Synopsys synthesis
EPOCH P&R
HP26g CMOS standard-cell library
sometimes MOSIS fab

Advanced Physical Design (next year) (ECE 652):

Mentor Graphics Design Architect
SmartModels for virtual prototyping

Mentor Graphics MCM Station
several persons/project
MIDAS fab

2. Do you encourage the actual fabrication of designs for beginning classes?
Yes, for ECE 651.

3. What experiences have you had in integrating research and education in your use of MOSIS?
I try to have these tightly coupled. I train potential researchers in the classes and I assign projects based on research interests. I demo/show classes projects what we have done for research. I usually try something new first using researchers and then put it in the classes but sometimes this is reversed.

4. What suggestions for future services do you have that would enhance the interest in use of MOSIS?
Another Professor in my dept. would like to do analog and/or mixed signal projects in classes like he already does for research. He may also want to use GaAs.

We have used MIDAS for a research project and now plan to use it in a course next year.
We have talked about using MEMS/MUMPS in a future course.

A. Role of VLSI and MOSIS in an Educational Setting

A1. Where is MOSIS used?
For introductory projects which are designed manually.

For mixed-signal or submicron layouts which are not modeled adequately.

For any project designed manually or automatcially which will be inserted into a system, not just a stand-alone tester.

A2. What is the educational value of MOSIS for schools?
Highly motivating for students to receive practical experience in experimental system building.

B. Fabrication vs. Simulation

B1. What is the educational value of a completed design (hard chip)?
Brings real-world experiences and motivation to the academic world. Probably doubles the interest level in a class.

B2. Do we really need to fabricate chips for elementary classes?
Yes, but just for my custom class whose enrollment is declining. Most of my students choose the FPGA class instead.

B3. To what extent should virtual prototyping be used, especially in beginning classes?
Thorough simulation should always precede fabrication but not totally replace physical prototyping.

C. MOSIS in VLSI Education

C1. How does group size influence the educational value to the student of the MOSIS experience?
Two persons per project is the right number. Any more than this waters down the effect and often leads to unbalanced teams that are hard to manage or grade.

C2. To what extent should the success rate of instructors' classes affect the priorities and funding of their subsequent classes?
Very little since so much is not under their control. Continuation should be granted provided good faith efforts are being made.

C3. What should the chip reports contain?
As much as possible.

C4. How should reports be accessible to others?
Information on the design is more interesting than the testing results of a particular implementation. The summaries distributed by CMP and CMC are very helpful. The test reports sent to MOSIS by others would not be much help.

C5. What does testing contribute to the designer's education?
Appreciation for real-world events and Murphy's Law.

D. The MOSIS Community

D1. Funding is tight, and likely to remain so for the foreseeable future. What steps may be taken to maintain and enhance the educational values MOSIS provides to US technical strength?
Encourage more use of FPGAs and prefabricated ICs (like Caverly's).

D2. It may be possible to organize an electronic bulletin board for Educational MOSIS, along the lines of the MEMS Bulletin Board. This would be a chiefly student/student information sharing network. What actions would be appropriate in this respect? How would such a network benefit the student and generate enthusiasm, better reporting and testing?
Great idea. Let's do it. The MOSIS Users' Group Newsletter (now the Microelectronic Systems Newsletter) does some of this but much more could be done.

THE UNIVERSITY OF UTAH, MOSIS AND NSF

Kent Smith

Tools:

We are presently using a variety of tools running on SUN and HP workstations for the design of VLSI chips both in classes and in research. A decision was made over a year ago to put a set of commercial tools in place for research and teaching and we have spent the past year getting these tools running. It has required new work stations, very large hard drives (approximately 100 Gigabytes of disk space) and a large commitment of time. The majority of the work required to get the tools running has now been completed but installation of new tools and upgrades of existing tools will continue indefinitely.

It was necessary to obtain licenses from the companies that supply the CAD tools. This has been a major effort and has taken a year to get everything in place. All of these companies have university programs where universities use the tools in research and teaching programs for a token of the full price that is charged commercial companies. These token charges, however, still amount to thousands of dollars each year and are presently financed by our research projects. The tools consist of:

ViewLogic: ViewDraw for schematic capture; ViewSim for gate level simulation; ViewTrace for graphical representation of the simulation

Synopsis: VHDL synthesis and simulation; Verilog synthesis and simulation

Cascade (Epoch): Place and route from netlists generated in ViewLogic and Synopsis; Floorplanning - Static timing analysis
Outputs CIF and GDSII
Interfaces to ViewLogic, Synopsis, HSPICE
Libraries for MOSIS Scaleable Rules, HP 0.6 m, Orbit 2m and 1.2m

Cadence: Virtuoso for composite layout and DRC; Dracula for extraction, ERC and LVS

HSPICE: Transistor simulation
GSI for graphical representation

Magic: Composite layout

Lager: Place and route, pad routing

Berkeley tools: Espresso, MISII, SIS, NOVA, etc. - Boolean optimization, state machine reduction, state encoding, etc.

The use of these tools have opened up opportunities that we did not have before, particularly in the area of applications of VLSI. For example, we can implement complete systems which include RAM, ROM, and standard cells for DSP applications. As a result of this capability, we have been exploring research opportunities using VLSI to solve problems in active noise cancellation, spread spectrum receivers, and SB/VQ systems. There have been significant advances in the theory related to DSP applications like these but until the advent of 2+ million integrated circuits, it has been difficult if not impossible to build significant systems. Several professors from the Electrical Engineering Department have become very interested in these projects. With the combination of their theoretical backgrounds and these new tools for VLSI design, we will be able to make a significant contributions in new classes.

AUTUMN QUARTER

I teach a three quarter sequence of classes on VLSI design. The first quarter is a project class. We introduce ViewLogic and Cascade for design of small projects. The class is divided up into groups of three students per group. Each group is allowed to design a chip for the 2.2 x 2.2 mm - 1.2m MOSIS small circuit. Students are required to pick a project on their own. We have been able to interest other professors in helping students to pick meaningful projects. For example, we had the following participation from other faculty members for projects in:

Computer Science - Content Addressable Memories, HP Runway Buss Controller

Electrical Engineering - Spread Spectrum Receivers, Noise Cancellation Circuits, Flat Panel Display Controllers, Adaptable FIR Filters

Bioengineering - Ultrasonic Scanners for Breast Cancer

There were a total of 15 projects in the Autumn 1995 Quarter. The complexity of the projects varied over a wide range but they all contained approximately 4,000-5,000 transistors or 1000 equivalent gates. The circuits were designed in ViewDraw using schematic capture with the standard libraries that are supported by Cascade. Circuits were made using pre-defined cells from the Cadence library including standard cells similar to 7400 series logic gates, buss cells such as counters, adders, multipliers, etc., memory cells including RAMs and ROMs, and input and output pad drivers. The circuits were imported into Epoch where they were placed and routed and checked for static timing. They were exported from Epoch to ViewSim where they were simulated at the gate level. CIF files were generated in Epoch for sending to MOSIS. The circuits were sent to MOSIS. Testing of the circuits will occur during Spring Quarter of 1996.

WINTER QUARTER

During the Winter quarter we gave the basic Carver Mead class where students are introduced to transistor models, composite layout and fabrication. Students are required to design two custom standard cells to add to the existing Cascade library. Custom design and DRC is done in Virtuoso, extraction is done with Dracula. Transistor simulation is done in HSPICE and gate level simulation is done in ViewSim. A small circuit containing the two custom standard cells along with other existing library cells is designed, checked and simulated using the tools. We do not intend to fabricate any of these circuits at MOSIS. We feel that the design experience with full custom layout, DRC, extraction, and both transistor and gate level simulations is all that is required. This type of experience will be valuable later to graduate students doing research for specific systems when they are required to build very specialized structures. For example, we are working on a large project with ARPA called Avalanche. Our graduate students and staff are designing full custom ICs for incorporation into the Cascade library.

SPRING QUARTER

This quarter is devoted to the design of analog/digital circuits. We cover timing analysis, design of analog components such as operational amplifiers and design of analog sub-system components. The sub-system components consist of circuits like A/D converters, D/A converters, delta-sigma modulators, switched capacitor filters, etc. We use Virtuoso for the composite layout of custom circuits and a U Utah-developed program called ACME/PPL for design of small systems containing both analog and digital circuits. We do

plan on fabricating some of these circuits so students can have the experience of testing analog circuits. In addition to this design class, we also hold a testing class during Spring Quarter where students are able to test the circuits that were designed during Autumn Quarter.

There is also a class offered on VHDL using the Synopsis design system for synthesis and simulation. We are still getting experience with the tools so we have not submitted VHDL-designed circuits to MOSIS for fabrication. However, we plan on having an advanced class next year with students who are experienced with all of our tools including Synopsis. The plan is to have a large team of 5-6 students to do a significant system design which would be fabricated at MOSIS using advanced class funding. We would like to involve outside companies with some of these designs. Companies that I have contacted are very interested in interacting with our students on projects that they see as important.

QUESTIONS THAT WERE POSED FOR THE WORKSHOP:

A. Role of VLSI and MOSIS in an Educational Setting

A1. Where is MOSIS used?

We use it both in classes and in our research. Students design 1.2 micron small MOSIS chips in our classes. Students and staff members design 1.2 micron small MOSIS chips and 0.6 micron HP chips for our research projects.

A2. What is the educational value of MOSIS for schools?

The real value is in acquainting students with the limitations and capability of state-of-the-art ICs. Fabrication of small systems using commercial CAD tools gives students valuable experience.

B. Fabrication vs. Simulation

B1. What is the educational value of a completed design (hard chip)?

The value comes at three different stages. (1) by testing the final part, they get first hand experience about timing, tester limitations, etc. and (2) they get the thrill of seeing their own circuit work. (3) they get the significant experience of finishing a chip for fab and getting ready for the testing.

B2. Do we really need to fabricate chips for elementary classes?

We think that there can be two kinds of elementary classes, one for custom layout and one for small system design. The primary value will be in the fabrication of new, unique systems, not in the design and fabrication of circuits that have been built many times before.

B3. To what extent should virtual prototyping be used, especially in beginning classes?

We believe that custom design of small ICs such as a JK flip/flop should only be done with virtual prototyping since components of this type are already available. The real value is in designing their own systems.

C. MOSIS in VLSI Education

C1. How does group size influence the educational value to the student of the MOSIS experience?

Work in industry and research work at universities is done as a team effort. A group of 2-3 people for small system designs is near optimal since it acquaints students with real-life challenges of group interaction. Two students are definitely better for custom layout of small projects but system design requires talents in different areas. With three students, I can have one student responsible for system level design, one for detailed circuit design and one for testing. With the present funding from NSF, I find that three student teams work very well and practically the only way I can do small systems with our CAD tools.

C2. To what extent should the success rate of instructors' classes affect the priorities and funding of their subsequent classes?

All of our chips work as designed so the success is good. The only problems that occur are in inadequate simulation. We believe that being able to build small systems with the 1.2 micron small chips from MOSIS for 3 students is a very wise use of funds.

C3. What should the chip reports contain?

We require an 8 page report including title page, abstract, text, figures, references, etc. for beginning classes and a 12 page report for experienced circuit designs. Completeness of the report is of paramount importance. Reports are graded for spelling and grammatical errors. The report contains (1) Title Page (a page by itself) (2) Abstract (no more than a 1/2 page) (3) System preview including motivation for designing the chip (4) Implementation and engineering considerations (bulk of the report) (5) Specifications including functional, timing, electrical, and environmental, temperature. (6) Tradeoffs: architectural and circuit tradeoffs, I/O considerations, floor-planning and interconnect approaches (7) Timing and Critical Paths (8) Block diagrams, logic/circuit diagrams, and algorithms. (9) Final layout plot (10) Brief simulation details (11) What you plan on doing for testing part and (12) Chip statistics: die size, total power, number of transistors, etc.

C4. How should reports be accessible to others?

The reports should be widely available. We have found that a good way is to have a contest. The University of Utah and the University of Michigan work together on a “best design” contest. **We would like to extend an invitation to others to join us.**

C5. What does testing contribute to the designer's education?

Testing is very important and should be required. Students learn as much about design when testing as when they are actually doing the design.

D. The MOSIS Community

D1. Funding is tight, ..etc

I think that we should encourage the use of commercial CAD tools at universities and the design of small systems at the undergraduate level.

D2. It may be possible to organize an electronic bulletin board …

A web page from each university talking about their experience would be a great idea.

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1. BACKGROUND

The Electical Engineering Department at UVa is a relatively small department with a faculty of approximately 18. The Department offers an undergraduate degree in electrical engineering only but has several areas of concentration. The concentration areas that use all or part of the VLSI sequence are computer engineering and applied electrophysics (semiconductors, optics, and microwaves). Each year, the department graduates approximately 30 "computer engineers" and 20 "electrophysists". In addition, the engineering school contains a separate Department of Computer Science of approximately 18 faculty. A number of these students take part of the VLSI sequence also and a "tools" course is offered by this faculty. Numerous joint research efforts are underway between the two departments. Finally, interaction takes place between the EE Department and the Materials Science and Engineering Department in the areas of device characterization and fabrication.

2.0 COURSES AND TOOLS

Six courses constitute a complete VLSI "program". These courses are:

(1) EE 435 Computer Organization and Design (UG)
(2) EE 436 Advanced Digital Design (UG)
(3) EE 563 Introduction to VLSI (UG and Grad)
(4) EE 564 Microelectronic Integrated Circuit Fabrication (UG and Grad)
(5) EE 507 Analog Integrated Circuits (UG and Grad)
(6) CS 851 VLSI Algorithms (Grad)

The reality of the situation is that since we do not have a specific VLSI program or degree, the students in the undergraduate program interested in VLSI take EE 435, EE 436, and EE 563 and either EE 564 or EE 507. Typically, graduate students with emphasis in VLSI systems will take EE 563, EE 564, EE 507, and CS 851. It is assumed that the material in at least EE 435 is familiar to the student. A Design experience to some level is included in each course.

(1) EE 435 Computer Organization and Design

Tools: Mentor Graphics Design Architect, Quicksim, and VHDL System-1076 Environment: Sun servers and X-terminals Results: Simulation of a microprocessor **Description**: The course introduces the student to the integration of the concepts of computer organization. Extensive use of simulation is used for verification. (30 students)

(2) EE 436 Advanced Digital Design (UG)

Tools: Mentor Graphics Design Architect, Quicksim, Autologic, and VHDL System-1076, Logic Modeling, Actel FPGA tools, and Minc PLD Synthesis Tool Environment:

Sun servers and X-terminals, Hewlett Packard Logic analyzers Results: Implementation of an special 8-bit microprocessor system using FPGAs
Description: The course is essentially a rapid prototyping course. It also introduces some advanced topics in digital switching systems. The students use commercial tools, Actel FPGAs and PLDs. Groups of three are used and team design is emphasized. (30 students)

(3) EE 563 Introduction to VLSI (UG and Grad)

Tools: UC/Berkeley Magic and Mentor Graphics IC Station Environment: Sun servers and X-terminals Results: Implementation of a "game" in a 2.0 micron MOSIS Tiny Chip
Description: The course introduces the student to the basic concepts of VLSI systems design. It covers the gamit from transistor design to systems issues. All students do the same project in groups of two. Testing is performed using a special fixture or using an HP 82000. (20 students)

(4) EE 564 Microelectronic Integrated Circuit Fabrication (UG and Grad)

Tools: Silvaco Athena (2-D Process Modeling) and Atlas (2-D device sim.) Environment: Sun servers and X-terminals, Class 10,000 clean room Results: Simulation of MOS processes and personal fabrication (in-house) of a MOS FET
Description: The course introduces the student to fabrication techniques. Significant simulation of the entire process is done and a device is built by each student in a cleanroom at UVa. (20 students)

(5) EE 507 Analog Integrated Circuits (UG and Grad)

Tools: HSPICE, Environment: Personal computers, Results: Simulation of numerous analog devices **Description**: The course introduces the student to analog integrated circuit design issues. Extensive use of simulation and simulation only is used. The student perform individual projects. (15 students)

(6) CS 851 VLSI Algorithms (Grad)

Tools: None; Environment: Sun servers and X-terminals; Results: Physical layout software tool
Description: The course gives a broad introduction to the field of VLSI circuit layout from an algorithmic point of view. The students work individually and develop a software tool. (10 students)

2.0 Do you encourage the actual fabrication of designs from beginning classes?

I strongly encourage the fabrication of "something" in the beginning courses. I think that the actual fabrication is an excellent motivation tool. Our students really like getting a design fabricated.

3.0 What experiences have you had in integrating research and education in your use of MOSIS?

A number of the research efforts onging use the MOSIS facility. The courses allow use to train the students on the tools that we use for the research efforts. Also, undergraduates often work on research efforts with the graduate students, thus needing a common set of tools and techniques. MOSIS is absolutely essential for our research efforts.

4.0 What suggestions for future services do you have that would enhance the interest in the use of MOSIS?

I think that the main limitation for the expansion of the MOSIS use is the availability of "good" libraries for the various technologies. The ITD cells have worked well but need to be updated for new technologies. Also, we need to get better integration of the libraries into the commercial tools. We want to be able to do standard cell design with MOSIS and commercial tools.

A. Role of VLSI and MOSIS in a Educational Setting

A.1 Where is MOSIS used? Where should it be used?

At UVa, MOSIS is used for two purposes. The first is for
instructional purposes in the introductory course in VLSI. As mentioned earlier, I think that fabrication is important in this area. Second, MOSIS is important to use for the development of experimental systems for our research efforts. It is invaluable in this context since industry will not provide such support directly.

A.2 What is the educational value of MOSIS for schools?

I think that the fact that a real chip will result is an extremely important motivator for the students. Also, the physical contraints that the actual implementation provides can not be underestimated! Also, since no changes can occur, the need for extensive virtual prototyping is reenforced.

B. Fabrication vs. Simulation

B.1 What is the educational value of the completed design (hard chip)?

Same answer as A.2.

B.2 Do we really want to fabricate chip for the elementary classes?

Since our first class contains a large project and has a systems flavor, fabrication is important. It is especially important for the undergraduates.

B.3 To what extent should virtual prototyping be used, especially in beginning classes?

Since the design is going to be constructed, extensive simulation of the entire system is critical. Since the students will be testing the chip, he/she needs to know it completely. I think that we need to make sure that we are all defining virtual prototyping the same way, however.

C. MOSIS in VLSI Education

C1. How does group size influence the educational value to the student of the MOSIS experience?

To some extent, it depends on the size of the project. Team issues are important for the students to discover. Two or three per group is fine. The groups should not exceed three. Also, it is important that all of the members of the group experience the entire process to some level.

C2. To what extent should the success rate of the instructors' classes affect the priorities and funding of their of their subsequent classes?

I am not sure how "success" is being defined. I think that all of the reports should be filed. I think that there should be some interaction with the organization that is always unsuccessful so that this organization can learn from others. I do not think that you should cut off an institution because of some arbitrary failure rate.

C3. What should the chip reports contain?

I am not interested in the success or failure of the project. As an instructor, I would be interested in the project description so that I could use it or some of my students could use it.

C4. How should reports be accessible to others?

Placing the information on the WWW is fine.

C5. What does testing contribute to the designer's education?

Testing is critical. Without the testing cycle, fabrication is unnecessary. If there is a problem, the debugging process is very educational. Even the process of testing is educational since not all "signals" are accessible. Organization and thought is required.

D. The MOSIS Community

D1. Funding is tight, and likely to remain so for the foreseeable future. What steps may be taken to maintain and enhance the educational values MOSIS provides to US technical strength?

Accountability is important. Even though I think that the actually "failure" rate is not the complete metric, the users should contribute something to the process. Such items as projects, instructional material, etc. could be contributed. Also, I am not convinced that it has to be completely free. I think that the users can actually pay something for the opportunity to use it. We buy other lab supplies.

D2 It may be possible to organize an electronic bulletin board for Educational MOSIS, along the lines of the MEMS Bulletin Board.

Sounds like an excellent idea.

VLSI Courses, VLSI Laboratory

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The EECS Dept. offers three undergraduate programs Electrical Engineering, Computer Engineering, and Computer Science, and an extensive graduate program. The following is list of the undergraduate and graduate VLSI courses in EECS:

Undergraduate
- EE126 VLSI Design and Simulation
- EE127 VLSI Fabrication Techniques
- EE128 Testing of VLSI circuits
- EE162 Design of Switching systems II
- EE165 Laboratory

Graduate
- EE213 Design of VLSI Circuits
- EE214 VLSI Design
- EE218 Analog VLSI circuit Design
- EE317 VLSI for DSP systems

In addition there is an extensive MEMS research at GWU, and we will have very soon MEMS courses added to the program.

1.What tools and procedures are you using?
The courses EE126-EE128 are required courses for the computer engineers, and are technical electives for other undergraduate programs. The two courses are one year sequence introductory courses to VLSI design and Testing. In EE126, the students design custom digital cells using MAGIC (2 persons/project), and recently we are trying to use CADENCE analog artist. The designs are sent to MOSIS for Fab using TinyChips during the winter break. The Chips are tested in the sequel course EE128, where the students learn about DFT techniques and faults in CMOS circuits. The students use advance testing equipment (Tektronix LV500), Hilevel testing machine, and a variety of logic analyzers. EE127 is introduction to Microelectronics fabrication techniques. EE162-EE165 introduce the students to the semicustom ASIC design using FPGA and using XILINX (2 persons/project). CAD tools used are ABLE (Data I/O) HDL, XILINX PC software. The graduate course EE213 uses CADENCE tools where students use Verilog HDL to learn design environment, and design architecture. EE 214 is an advanced ASIC design using synthesis, and using CADENCE and Synopsys CAD tools (sometimes MOSIS fab). EE218 Analog VLSI circuit Design, Analog and Mixed design, low power design, students are required to complete a design project using MAGIC, and SPICE, and recently we are trying to use CADENCE Analog Artist; designs are submitted to MOSIS for fab. Designs include many research topics; testing of the fabricated design is done using automated PC station.

2. Do you encourage the actual fabrication of designs for beginning classes?
YES for EE126 and EE128 it is required. It is also required for the analog design EE218 course. For other Digital design courses it is optional, but many times students request fabrications.

3. What experiences have you had in integrating research and education in your use of MOSIS?
Many of my research projects started as a class project which evolved as a research project. In fact the ability to measure physically the design allows the student to think about new and novel ways to improve his design. I usually try to direct the class projects toward recent topics of research .

4. What suggestion for future services do you have that would enhance the interest in use of MOSIS?
As I have been active in MEMS research I would like to see more usage of MEMS by the MOSIS community. Also I would like to see smaller feature sizes with reasonable prices.

A1. Where is MOSIS used?
In EE126 Introductory to VLSI design, and in EE218 Analog VLSI design, and in research projects, ivolving mixed - signals, where modeling is difficult.

A2. What is the educational value of MOSIS for schools?
It is the key factor for students to learn VLSI design basics, invaluable experience for students to go to work for the industry. This is especially important for schools which don't have access to a process facility.

B1. What is the educational value of a completed design (hard chip)?
Many of my students were hired by companies because of their experience with fabrication testing their own design. This is the real world experience which is very important for many ASIC designers.

B2. Do we really need to fabricate chips for elementary classes?
YES

B3. To what extent should virtual prototypying be used, especially in a beginning class?
Simulation is always important, but it cannot replace the physical device and the physical testing of the prototype in the laboratory.

C1. How does group size influence the educational value to the student of MOSIS experience?
Two students per project is the ideal size. I tried larger size group, but I had lots of problems.

C2. To what extent should the success rate of instructors classes affect the priorities and funding of their subsequent classes?
Very difficult to control for large class and complex designs, but mandatory testing of the design and meaningful results might help.

C3. What should chip report contain?
Design simulations, and Testing results using laboratory equipment. A complete report is very useful, the current MOSIS format needs to be changed to be more thoughtful.

C4. How should reports be accessible to others?
MOSIS should publish yearly the projects titles received, and the institutes submitting the projects, and may be test results, and e-mail of liaison to contact for further information.

C5. What does testing contribute to the designers education?
Our students are required to test their chips, there are no designers in the real world who do

not test their design. It is a necessity for ASIC designer. It is also motivation for the students to carefully design and simulate their projects as testing is a part of the final grading.

D1. Funding is tight, and likely to remain so for foreseeable future. What steps may be taken to maintain and enhance the educational value MOSIS provides to US technical strength ?
Current funding is adequate. Possibly use old cheap technology to reduce the costs but tocertain limit.

D2. It may be possible to organize an electronic bulletin board for educational MOSIS, along the lines of the MEMS bulletin board.
Good idea. Give the students enthusiasm and could lead to better projects.